JUNE 2001 Rev. 1.2

8-BIT SINGLE CHIP MICROCOMPUTERS

GMS810 SERIES
APPLICATION NOTE

- GMS81004
- GMS81008
- GMS81016
- GMS81024
- GMS81032

Table of Contents

Chapter 1

Chapter 2

Appendix

CHAPTER 1. OVERVIEW

1. General Description

1) Object

This APPLICATION NOTE deals with application examples utilizing the special function of the GSM810 Series.
It has been compiled to assist programmer by providing application examples with circuit diagram, timing chart and program list.
Application examples in this notes should be tested by actual operation before being put to practical use.

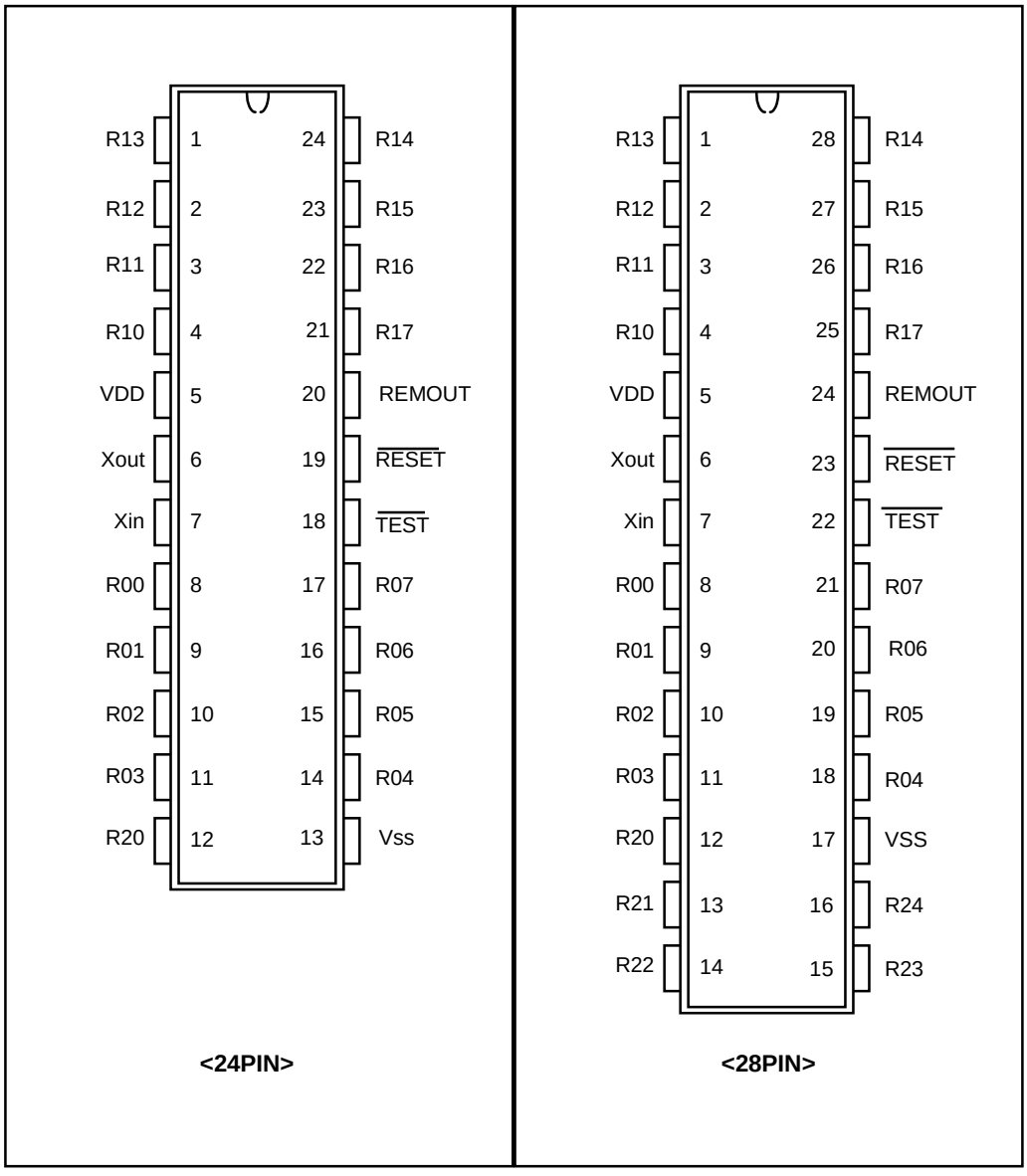
2) Architecture

The GMS810 Series is the high speed and low voltage operating 8-bit single chip microcomputers. This MCU contains G8MC core, ROM, RAM, input/output ports and five multi-functin timer/counters

 # FEATURES #

- ROM size . . . . . 16,384 Bytes(GMS81016)
  8,192 Bytes(GMS81008)
  4,096 Bytes(GMS81004)
- RAM size . . . . . 448 Bytes
- Instruction Execution Time . . 1us @4MHz
- Timer
  - Timer/Counter . . . . . 8Bit * 2ch
    . . . . . 16Bit * 1ch
  - Basic Interval Timer . . . 8Bit * 1ch
  - Watch Dog Timer . . . . . 6Bit * 1ch
- Power On Reset
- 2 Power Saving Operation Modes
  - STOP
- 8 Interrupt Sources
  - Nested Interrupt Control is Available
- Operating Voltage
  - 2.0~4.0V @2MHz
  - 2.2~4.0V @4MHz
- Low Voltage Detection Circuit
- Package
  - 24SOP/28Skinny DIP/28SOP
  - 24Skinny DIP (Under development)
- I/O Port
  - Input : 3
  - Output: 2
  - I/O : 21

3) PIN DIAGRAM



2 Explanation of Symbols

1) Operation

a → b	→	Transfer a to b
a ↔ b	→	Exchange a with b
+	→	Addition
-	→	Subtraction
×, *	→	Multiplication
÷, /	→	Division
∧	→	AND
∨	→	OR

(2) Register within the MCU

A	→	Accumulator
B	→	X Register
Y	→	Y Register
PSW	→	Program Status Word
SP	→	Stack Pointer
PC	→	Program Counter

(3) Flag within the MCU

C	→	Carry

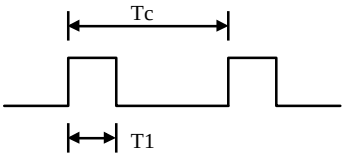
(4) Other Symbols

=	→	Equivalence
≠	→	Not equal
<, >	→	Comparison
#	→	Immediate data (hex., binary, decimal)
!	→	Absolute address
$	→	Current line address
:	→	Label
;	→	Comment
H, h	→	Hex. decimal
D.d	→	Decimal
B,b→	Binary	
Y	→	Yes
N	→	No
″	→	Character string
′	→	Operand
.	→	Bit position (ex> A.3 <-bit3 of A)
[ ]	→	Indirect addressing

3. Output Waveform

1) uPD6121G with simple repeat code

A single pulse, modulated with 37.91KHz signal at 455KHz



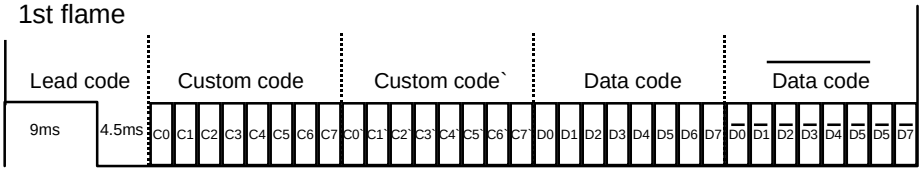
Carrier frequency

$f_{CAR} = 1/Tc = f_{OSC}/12$

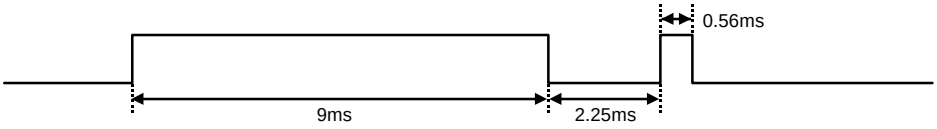
Duty ratio = T1/Tc = 1/3

- Configuration of Flame

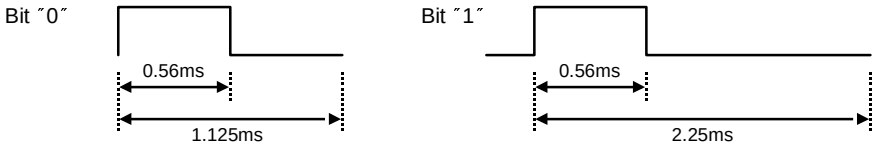
1st flame



- Repeat code

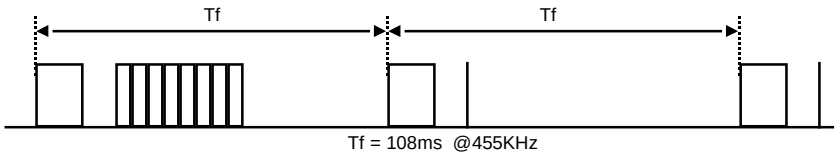


- Bit Description



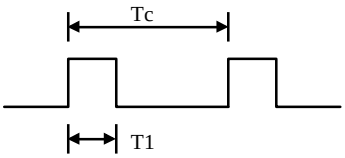
- Flame Interval : Tf

The transmitted waveform as long as a key is depressed



2) uPD6121G with full repeat code

A single pulse, modulated with 37.91KHz signal at 455KHz



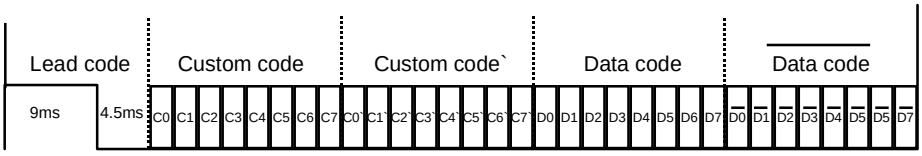
Carrier frequency

$f_{CAR} = 1/Tc = f_{OSC}/12$

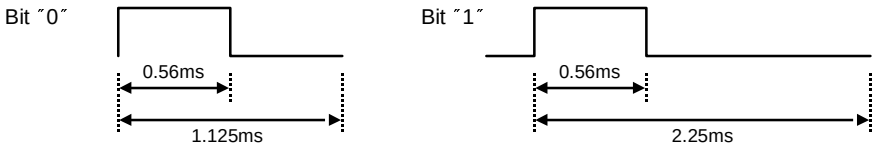
Duty ratio = T1/Tc = 1/3

- Configuration of Flame

1st flame

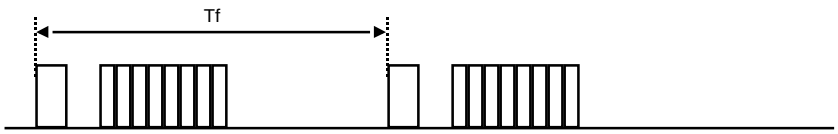


- Bit Description



- Flame Interval : Tf

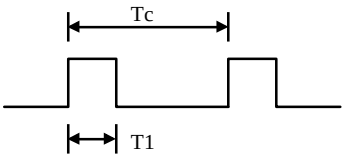
The transmitted waveform as long as a key is depressed



Tf = 108ms @455KHz

3) TC9012F/9243

A single pulse, modulated with 37.91KHz signal at 455KHz



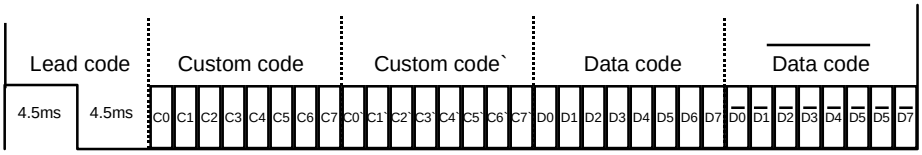
Carrier frequency

$f_{CAR} = 1/Tc = f_{OSC}/12$

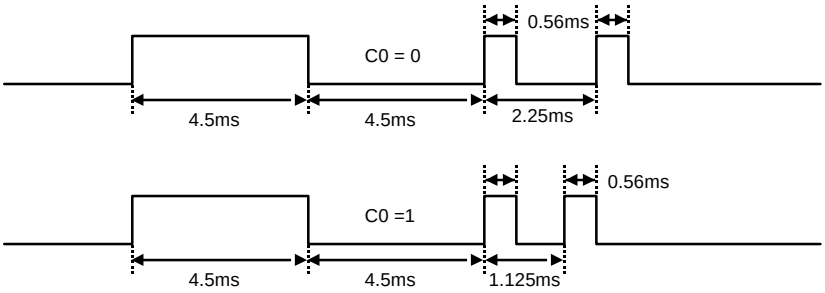
Duty ratio = T1/Tc = 1/3

- Configuration of Flame

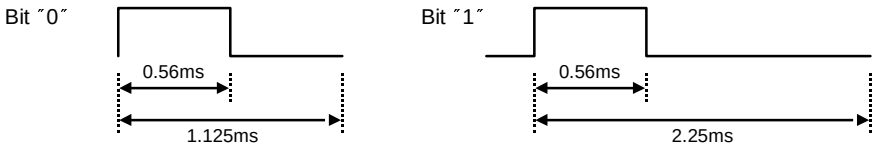
1st flame



- Repeat code

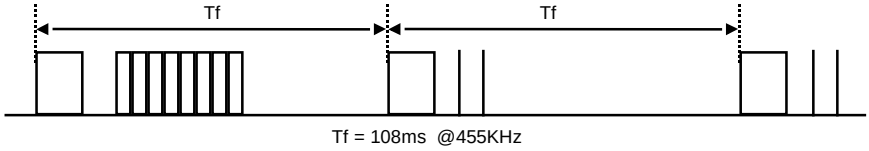


- Bit Description



- Flame Interval : Tf

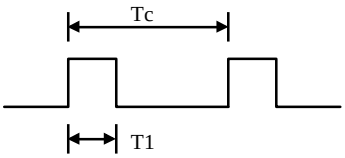
The transmitted waveform as long as a key is depressed



Tf = 108ms @455KHz

4) M50560-001P

A single pulse, modulated with 37.91KHz signal at 455KHz



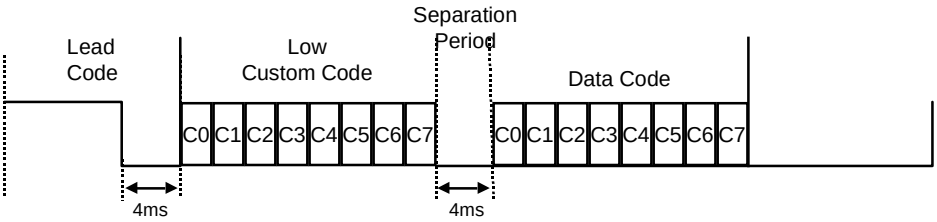
Carrier frequency

$f_{CAR} = 1/Tc = f_{OSC}/12$

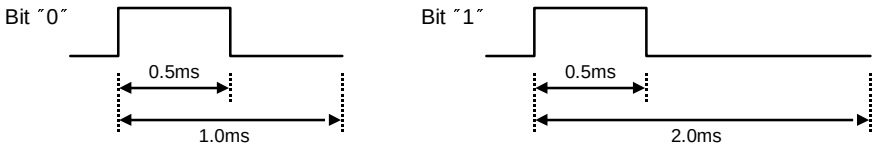
Duty ratio = T1/Tc = 1/3

- Configuration of Flame

1st flame

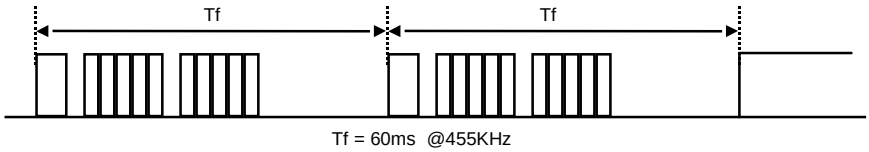


- Bit Description



- Flame Interval : Tf

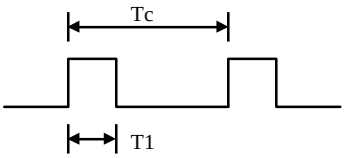
The transmitted waveform as long as a key is depressed



Tf = 60ms @455KHz

5) LC7461M-C13 with simple repeat code

A single pulse, modulated with 37.91KHz signal at 455KHz



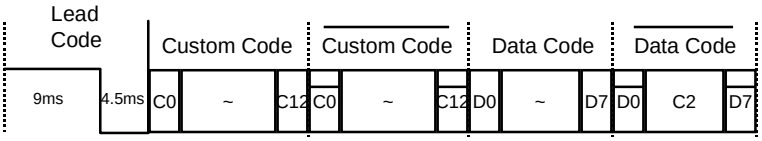
Carrier frequency

$f_{CAR} = 1/Tc = f_{OSC}/12$

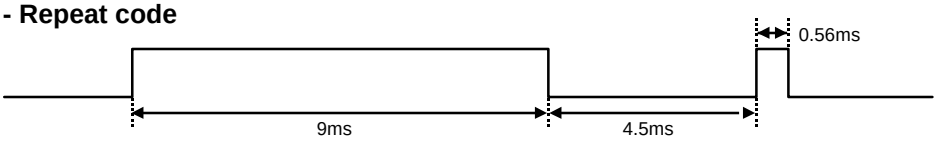
Duty ratio = T1/Tc = 1/3

- Configuration of Flame

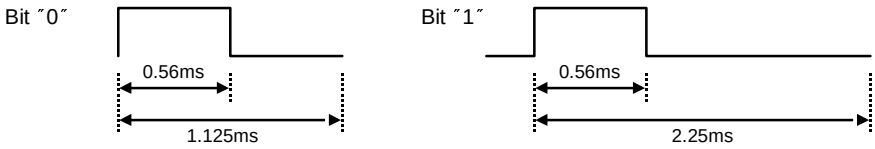
1st flame



- Repeat code

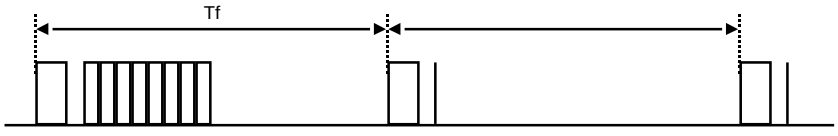


- Bit Description



- Flame Interval : Tf

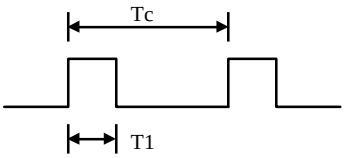
The transmitted waveform as long as a key is depressed



Tf = 108ms @455KHz

6) LC7461M-C13 with full repeat code

A single pulse, modulated with 37.91KHz signal at 455KHz



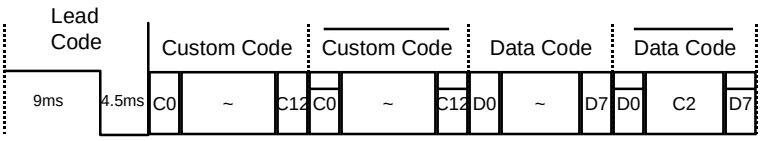
Carrier frequency

$f_{CAR} = 1/Tc = f_{OSC}/12$

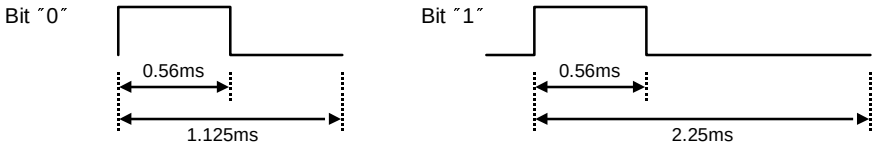
Duty ratio = T1/Tc = 1/3

- Configuration of Flame

1st flame

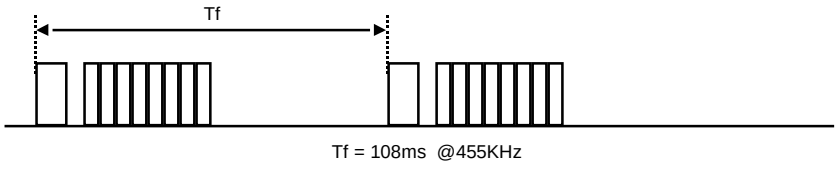


- Bit Description



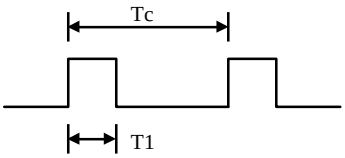
- Flame Interval : Tf

The transmitted waveform as long as a key is depressed



7) M3004 LAB1-Carrier

A single pulse, modulated with 37.91KHz signal at 455KHz



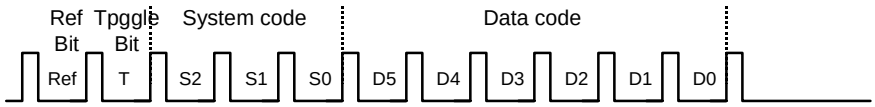
Carrier frequency

$f_{CAR} = 1/Tc = f_{OSC}/12$

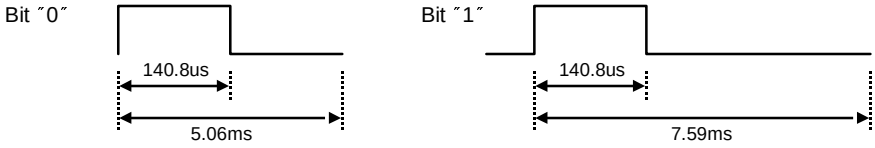
Duty ratio = T1/Tc = 1/3

- Configuration of Flame

1st flame

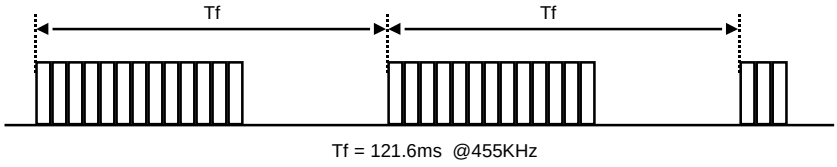


- Bit Description



- Flame Interval : Tf

The transmitted waveform as long as a key is depressed



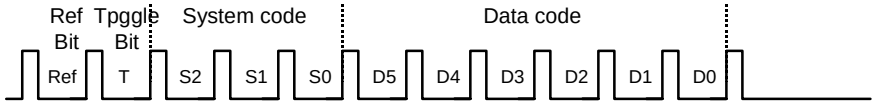
Tf = 121.6ms @455KHz

8) M3004 LAB1 - Flash

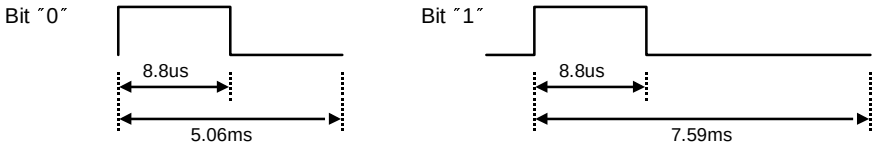
A single pulse at 455KHz

- Configuration of Flame

1st flame

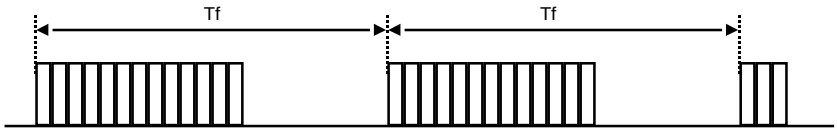


- Bit Description



- Flame Interval : Tf

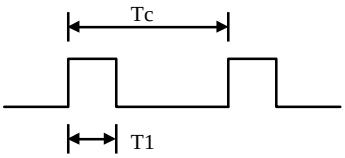
The transmitted waveform as long as a key is depressed



Tf = 121.6ms @455KHz

9) SAA3010(RC-5)

A single pulse, modulated with 37.917KHz signal at 455KHz



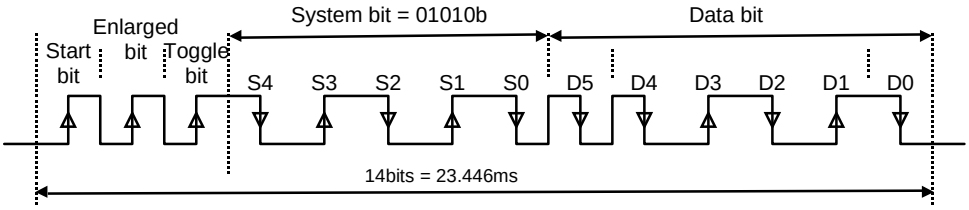
Carrier frequency

$f_{CAR} = 1/Tc = f_{OSC}/12$

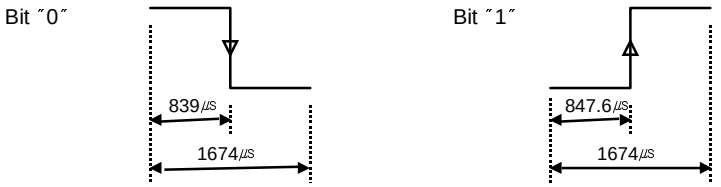
Duty ratio = T1/Tc = 1/3

- Configuration of Flame

1st flame

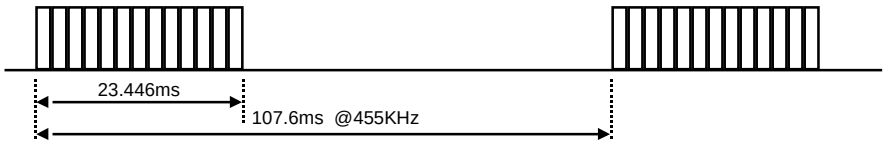


- Bit Description



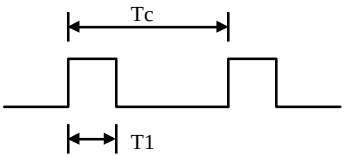
- Flame Interval : Tf

The transmitted waveform as long as a key is depressed



10) uPD1986C

A single pulse, modulated with 37.917KHz signal at 455KHz



Carrier frequency

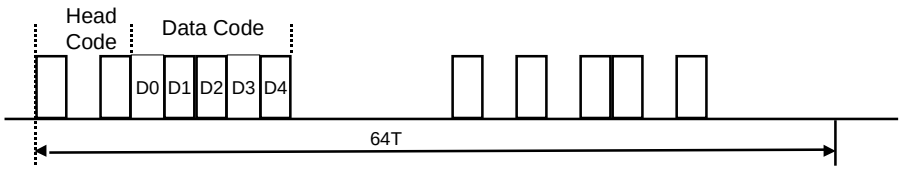
$f_{CAR} = 1/Tc = f_{OSC}/12$

Duty ratio = T1/Tc = 1/3

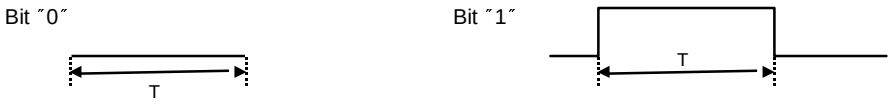
Time Unit = T = 43Tc

- Configuration of Flame

1st flame

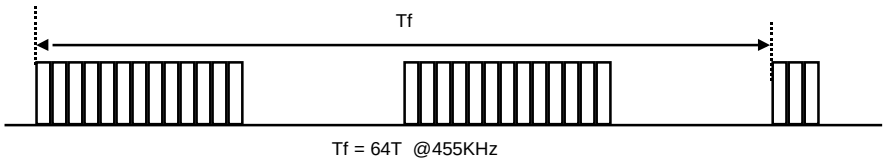


- Bit Description



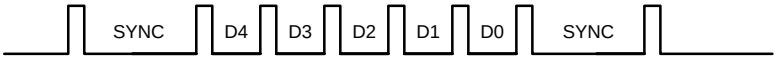
- Flame Interval : Tf

The transmitted waveform as long as a key is depressed

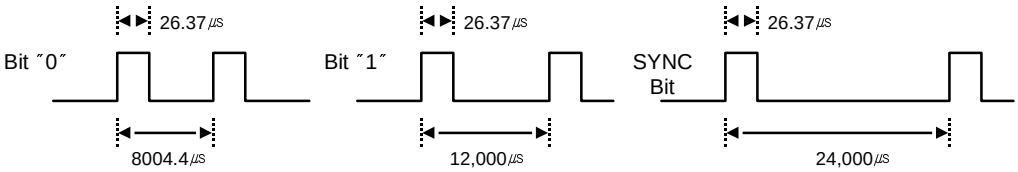


11) MV500 (4ms)

A single pulse at 455KHz

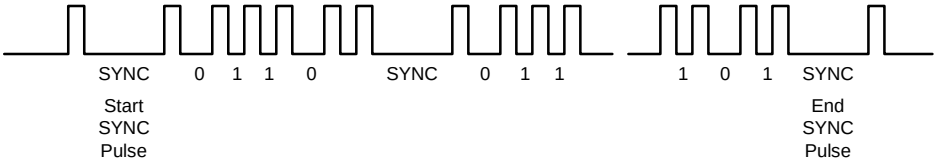


- Bit Description



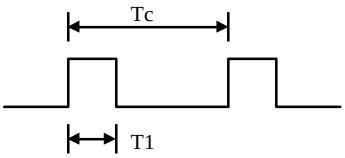
- Flame Interval : Tf

The transmitted waveform as long as a key is depressed



12) Zenith CG1

A single pulse, modulated with 40KHz signal at 480KHz



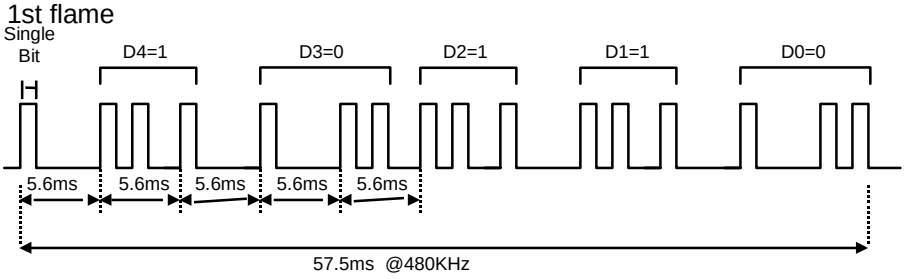
Carrier frequency

$f_{CAR} = 1/Tc = f_{OSC}/12$

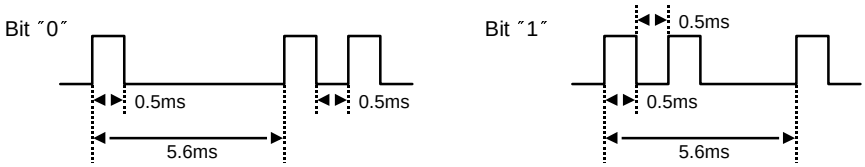
Duty ratio = T1/Tc = 1/3

- Configuration of Flame

1st flame

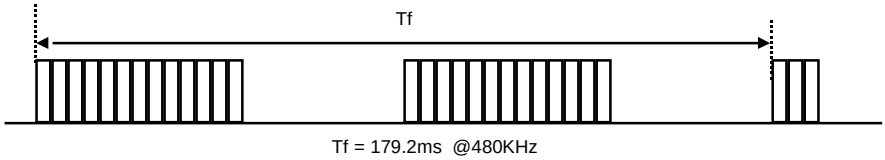


- Bit Description



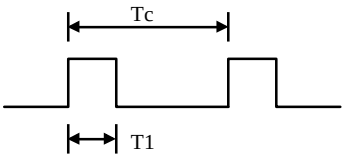
- Flame Interval : Tf

The transmitted waveform as long as a key is depressed



13) Zenith CG2

A single pulse, modulated with 40KHz signal at 480KHz



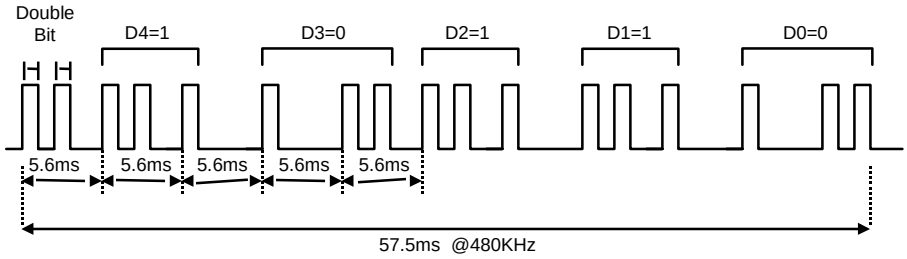
Carrier frequency

$f_{CAR} = 1/Tc = f_{OSC}/12$

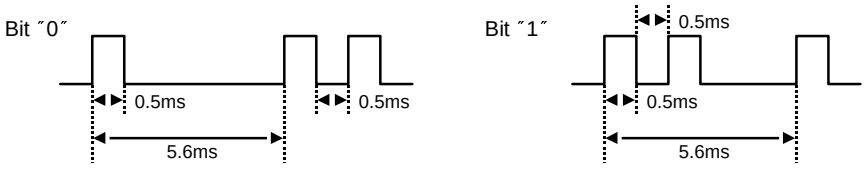
Duty ratio = T1/Tc = 1/3

- Configuration of Flame

1st flame

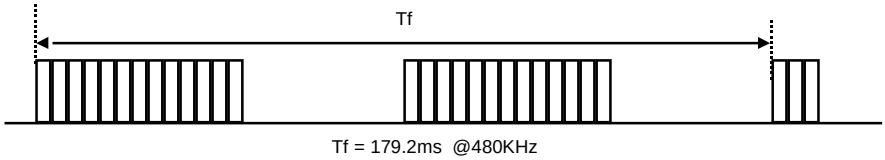


- Bit Description



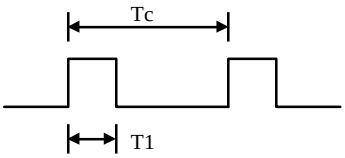
- Flame Interval : Tf

The transmitted waveform as long as a key is depressed



14) LR3715M

A single pulse, modulated with 37.917KHz signal at 455KHz



Carrier frequency

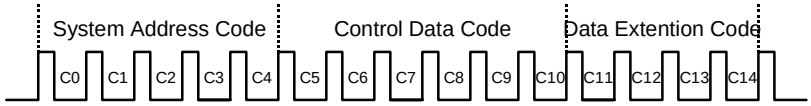
$f_{CAR} = 1/Tc = f_{OSC}/12$

Duty ratio = T1/Tc = 1/3

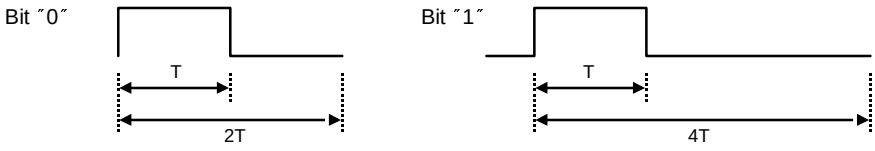
Time Unit = T = 10Tc

- Configuration of Flame

1st flame

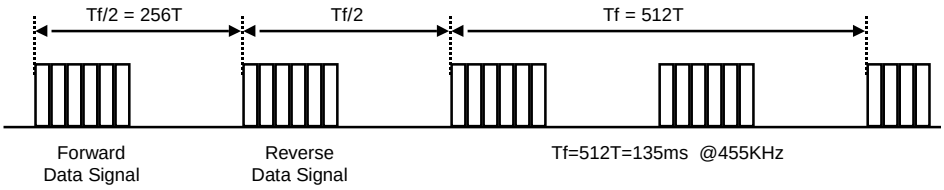


- Bit Description



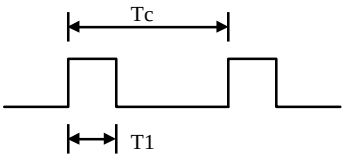
- Flame Interval : Tf

The transmitted waveform as long as a key is depressed



15) SONY - D7C6

A single pulse, modulated with 40KHz signal at 480KHz



Carrier frequency

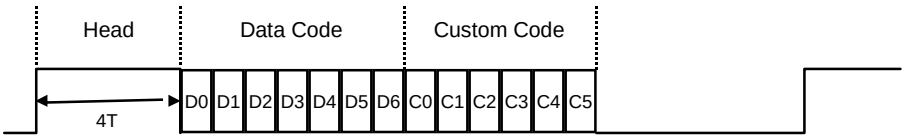
$f_{CAR} = 1/Tc = f_{OSC}/12$

Duty ratio = T1/Tc = 1/3

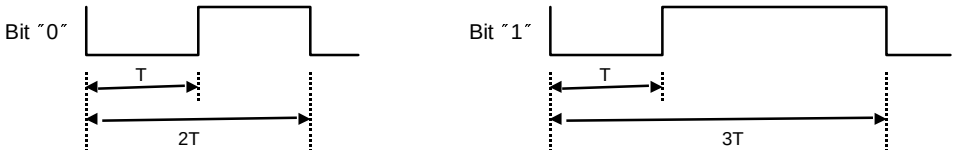
Time Unit = T = 24Tc = T

- Configuration of Flame

1st flame

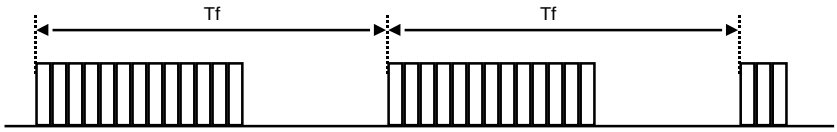


- Bit Description



- Flame Interval : Tf

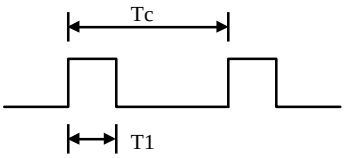
The transmitted waveform as long as a key is depressed



Tf = 45ms = 75T @480KHz

16) SONY - D7C8

A single pulse, modulated with 40KHz signal at 480KHz



Carrier frequency

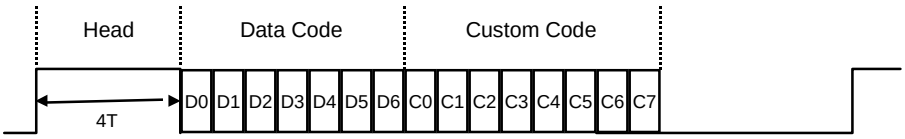
$f_{CAR} = 1/Tc = f_{OSC}/12$

Duty ratio = T1/Tc = 1/3

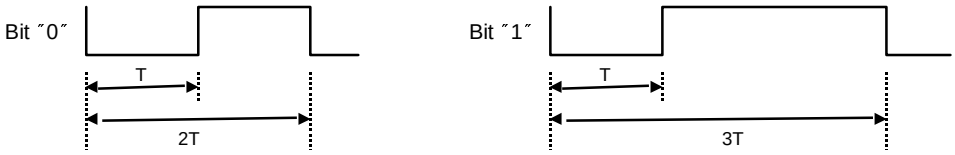
Time Unit = T = 24Tc

- Configuration of Flame

1st flame

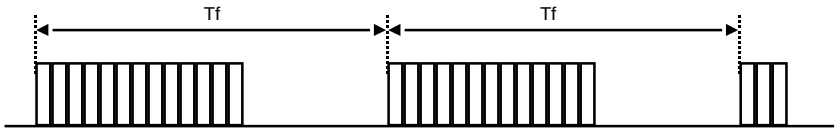


- Bit Description



- Flame Interval : Tf

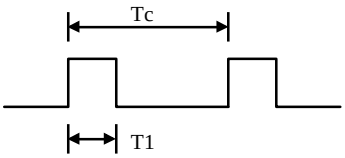
The transmitted waveform as long as a key is depressed



Tf = 45ms = 75T @480KHz

17) MN6014-C5D6

A single pulse, modulated with 56.875KHz signal at 455KHz



Carrier frequency

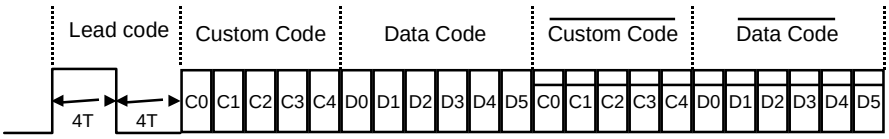
$f_{CAR} = 1/Tc = f_{OSC}/12$

Duty ratio = T1/Tc = 1/3

Time Unit = 32Tc = T

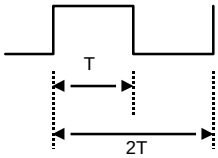
- Configuration of Flame

1st flame

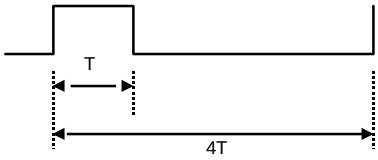


- Bit Description

Bit ˝0˝

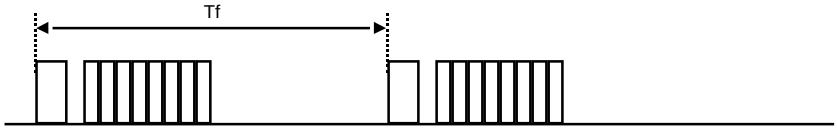


Bit ˝1˝



- Flame Interval : Tf

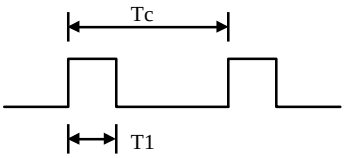
The transmitted waveform as long as a key is depressed



Tf = 101.3ms @455KHz

18) MN6014-C6D6

A single pulse, modulated with 36.6KHz signal at 440KHz



Carrier frequency

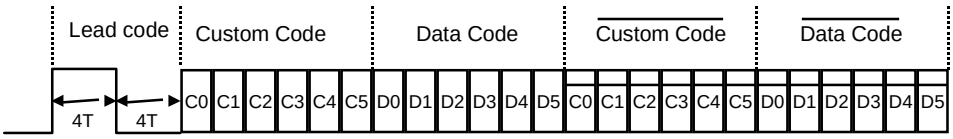
$f_{CAR} = 1/Tc = f_{OSC}/12$

Duty ratio = T1/Tc = 1/3

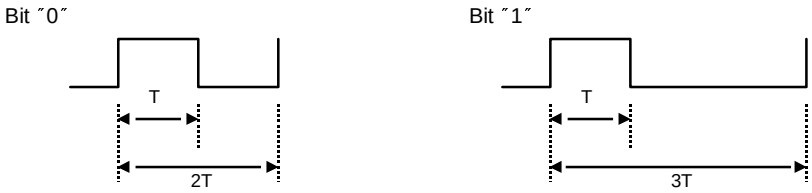
Time Unit = 32Tc

- Configuration of Flame

1st flame

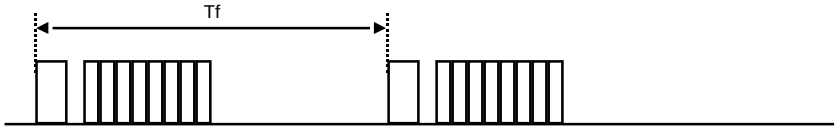


- Bit Description



- Flame Interval : Tf

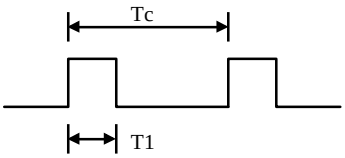
The transmitted waveform as long as a key is depressed



Tf = 120T = 104.7ms @440KHz

19) AEHA

A single pulse, modulated with 37.917KHz signal at 455KHz



Carrier frequency

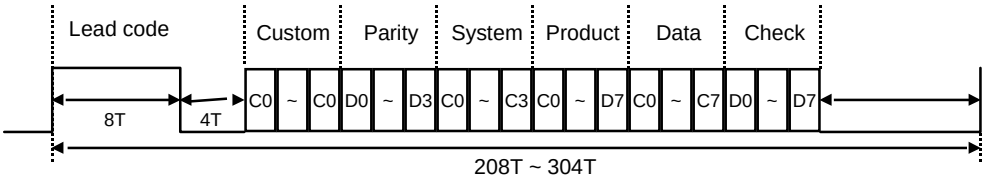
$f_{CAR} = 1/Tc = f_{OSC}/12$

Duty ratio = T1/Tc = 1/3

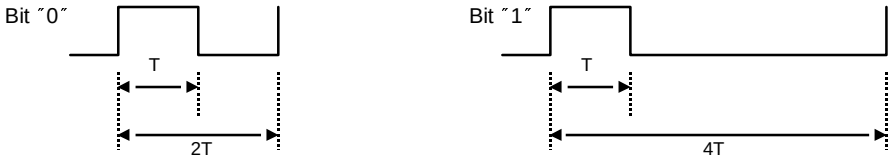
Time Unit = 16Tc = T

- Configuration of Flame

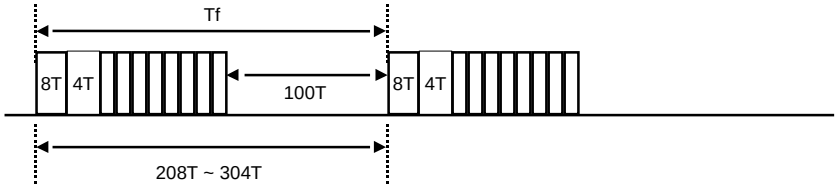
1st flame



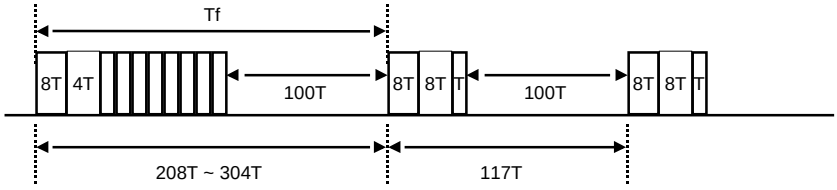
- Bit Description



- Normal Repeat



- Abbreviated Repeat

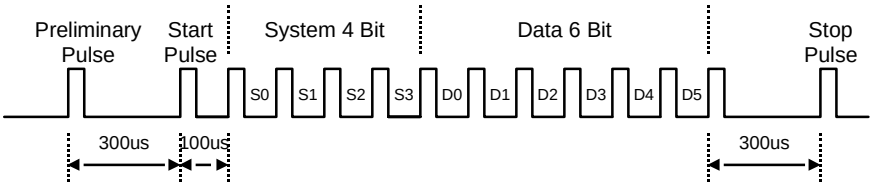


20) IRT1250

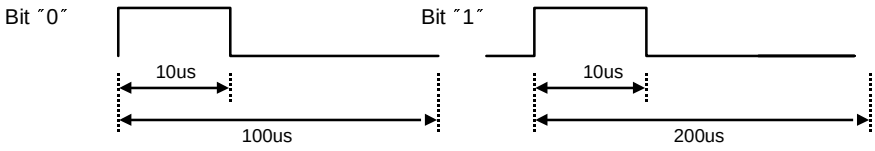
A single pulse at 600KHz

- Configuration of Flame

1st flame

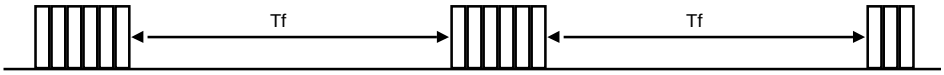


- Bit Description



- Flame Interval : Tf

The transmitted waveform as long as a key is depressed

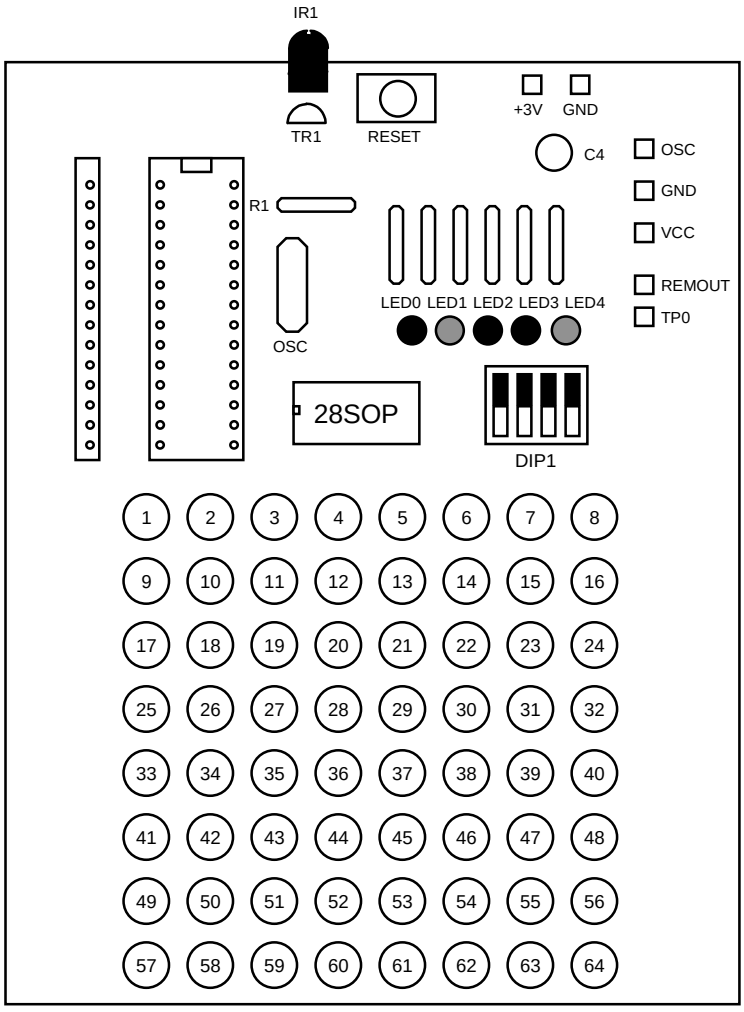


Tf=140ms @600KHz

4. USING OF DEMO BOARD

4-1. GS81016 DEMO BOARD

This demo board is used for supporting remote controller programming. Basic test pins such as remote out, oscillation, ports are provide. if is easy to know the key action and port status.

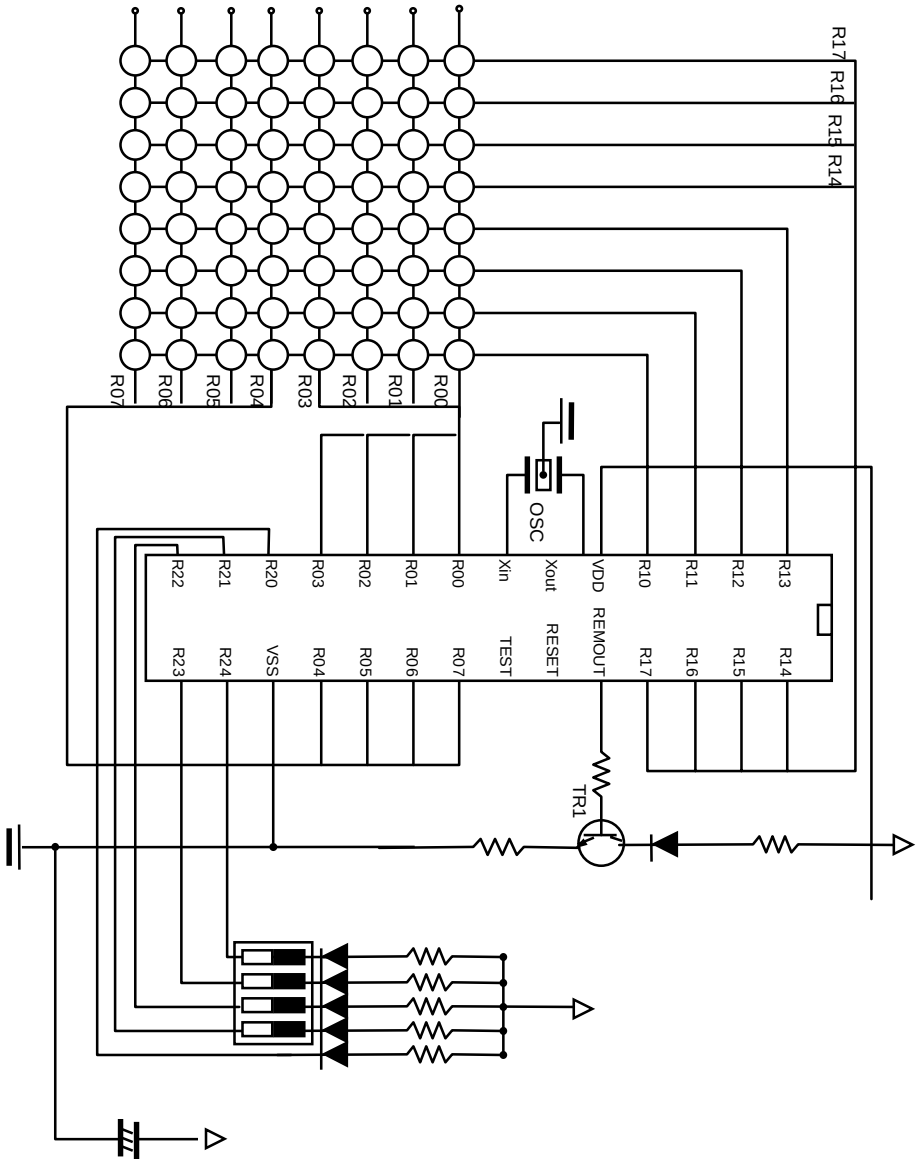


VCC : 3V
U1 : 28SDIP socket for OTP, MDS
TR1 : KN2222A (NPN) TR
IR1: SLR932A, SE303A-C
R5 : Emitter resistor
LED0~LED4 : R20~R24PORT
R0~R4 : LED resistor, 100ohm
DIP1 : LED selection dip
C1 : capacitor, 47uF16V
C2 : Reset capacitor, 100uF
C3~C4 : OSC capacitor
OSC : 4MHz
RESET : Reset Switch
TEST PIN

TP0~TP4 : R20~R24 test pin
VCC : Vcc test pin
REMOUT : Remote out test pin
OSC : Oscillator test pin
GND : Ground test pin

GMS810XX DEMO BOARD VER2.0

4-2. Circuit Diagram



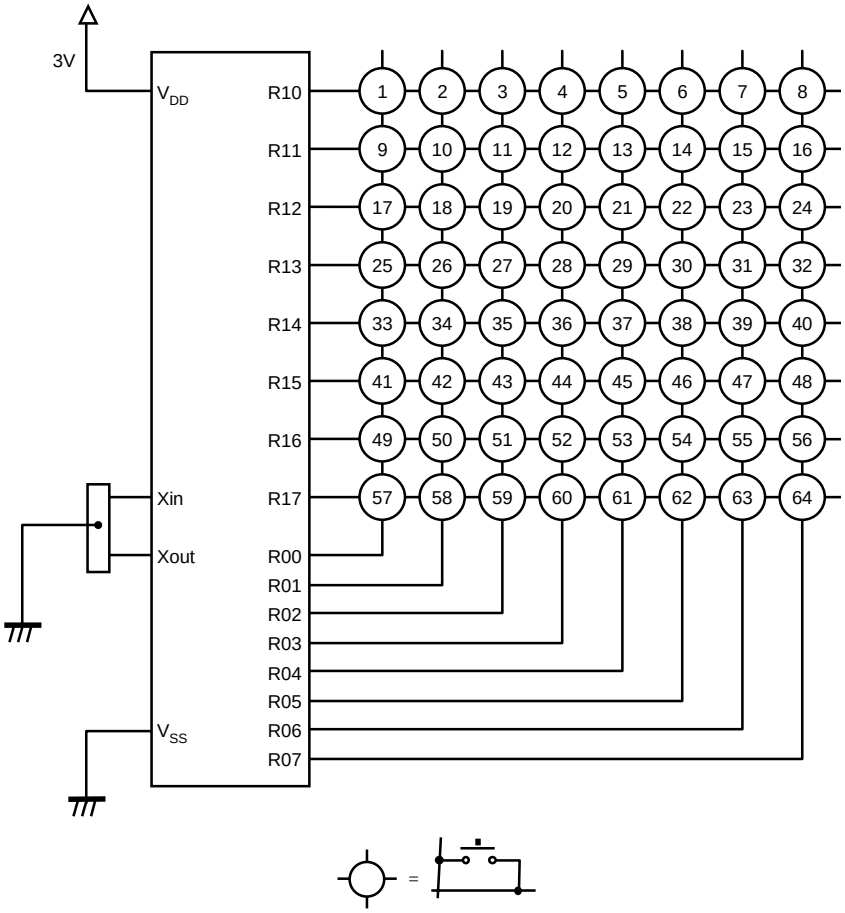
CHAPTER 2. APPLICATION EXAMPLE

1. KEY MATRIX SCAN

1-1. OVERVIEW

This program shows the method of scanning 8×8 key matrix and using timer interrupt.

1-2. HARDWARE DESCRIPTION



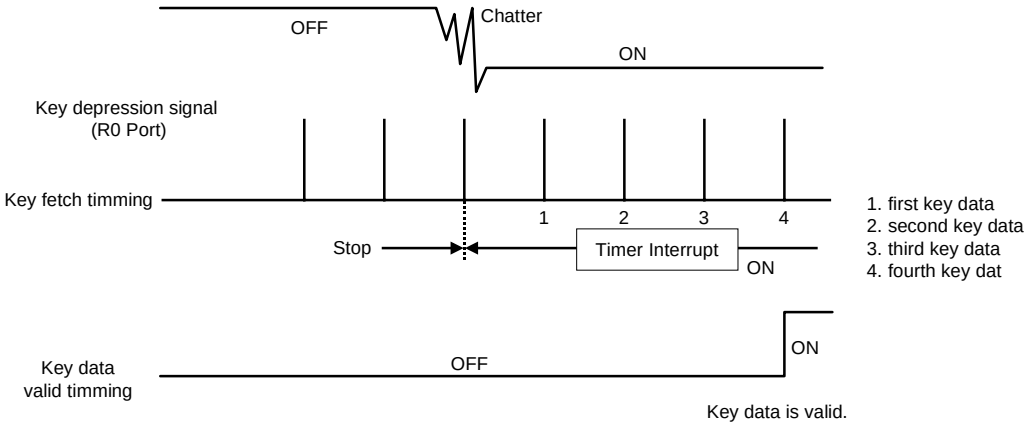
1-3. MCU Operation

Timer2 : 8bit, Source Clock = 4MHz, Interrupt cycle = 10ms

1-4. Pin Function

Pin No.	Name	I/O	Description
8	R00	Input	Key Data Input (1column)
9	R01	˝	˝ (2column)
10	R02	˝	˝ (3column)
11	R03	˝	˝ (4column)
18	R04	˝	˝ (5column)
19	R05	˝	˝ (6column)
20	R06	˝	˝ (7column)
21	R07	˝	˝ (8column)
4	R10	Output	Strobe Signal Output (1line)
3	R11	˝	˝ (1line)
2	R12	˝	˝ (1line)
1	R13	˝	˝ (1line)
28	R14	˝	˝ (1line)
27	R15	˝	˝ (1line)
26	R16	˝	˝ (1line)
25	R17	˝	˝ (1line)

1-5. H/W Operation

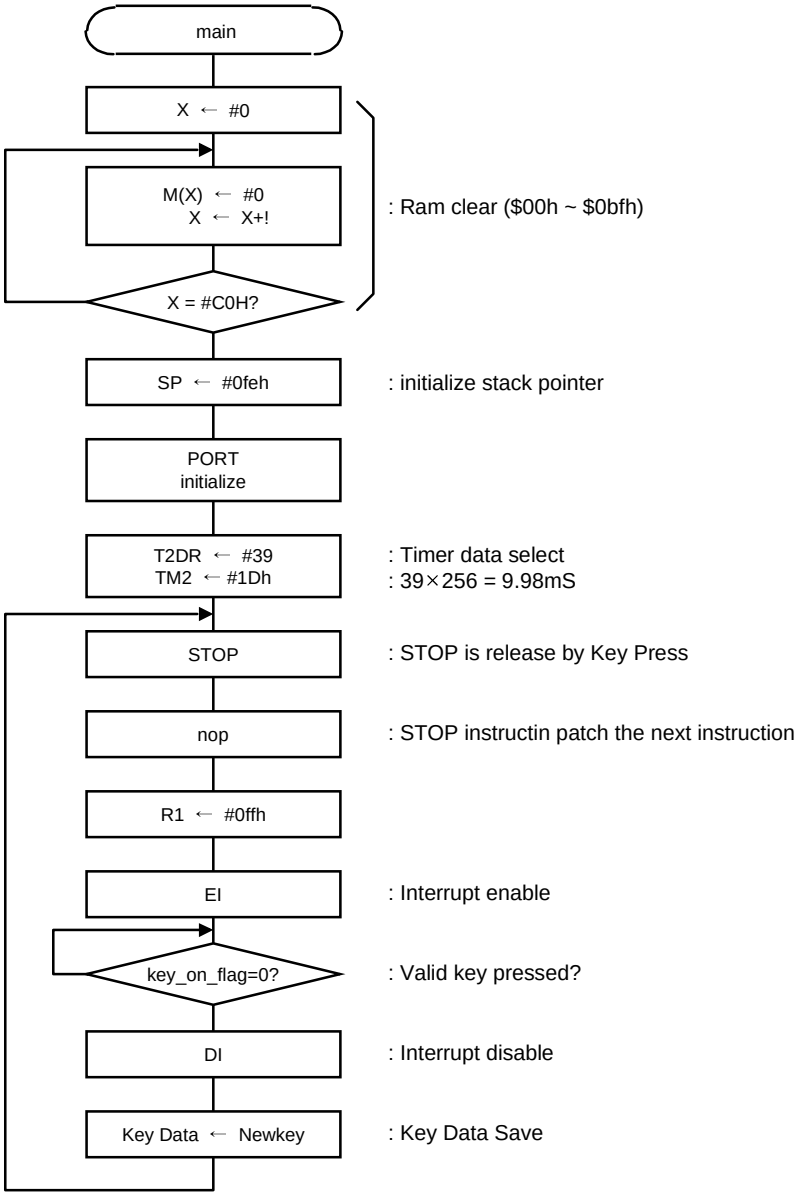


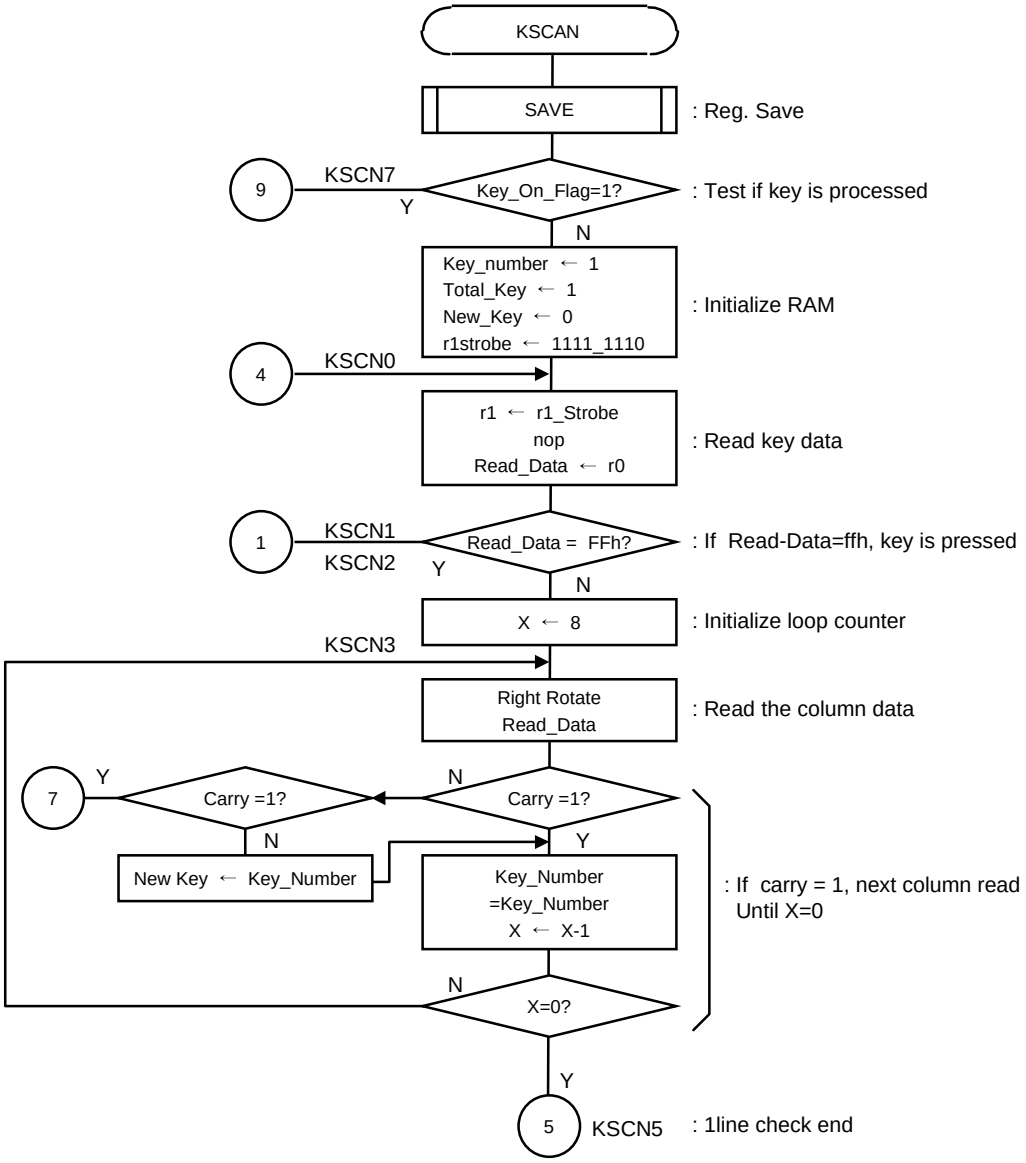
1-6. Software Description

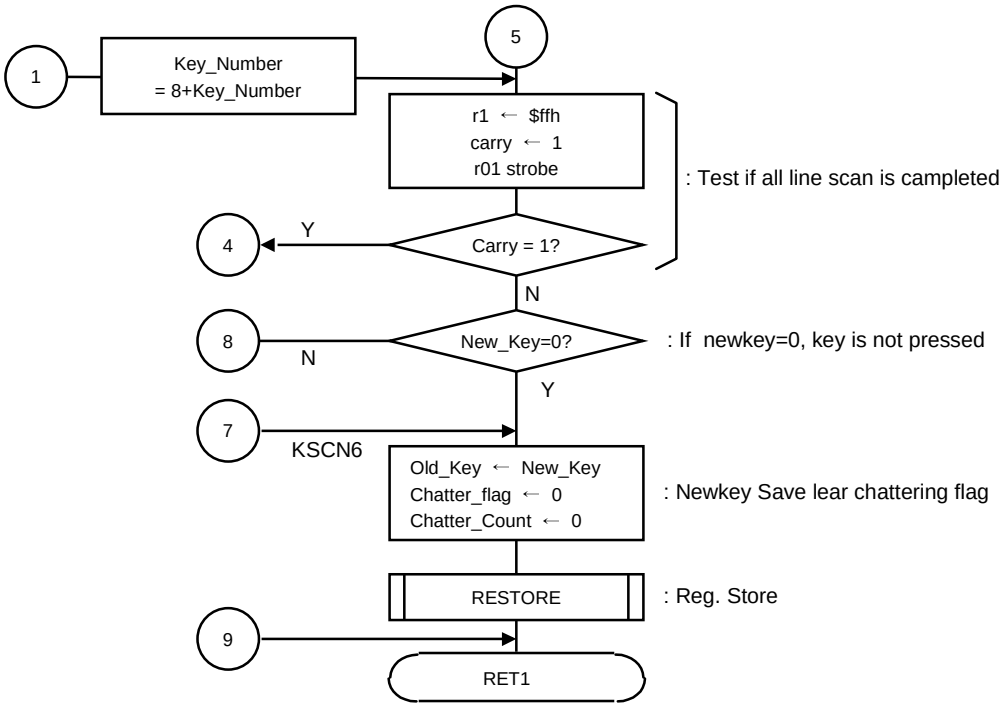
- Key scan is executed by every 10ms interrupt.
  At the beginning of key scan, key data valid/invalid flag (KEY-ON-FLAG) is checked to determine whether the valid key data has been processed or not.
- Strobe signal(high active) is output through port R1, and key scan data is fetched through port R0.
- Key scan data tested whether it is #FFh.
  If #FFh, no key is depressed and key scan for next column is executed. If not #FFh, some key is depressed and row of depressed key is tested. Key scan data is shifted 1 bit right 8 times. If Carry is 0, it means a key is depressed.
- Key data (KEY-NUMBER) is numbered from 1 to 64, based on position in 8*8 key matrix.
- TOTAL-KEY(RAM) is increment every time a key is depressed to check for chatter. If TOTAL-KEY(RAM) > 1, key scan is completed since it indicated two or more keys are pressed at the same time.
- Key data(NEW-KEY) is compared with previous key data (OLD-KEY).
  If they are same, chatter counter (CHATTER-COUNT) is counted up when chatter counter becomes 3, key data is valid.
- If key data is valid, KEY-ON-FLAG(RAM) is set to 1 and Newkey(RAM) contains valid data.

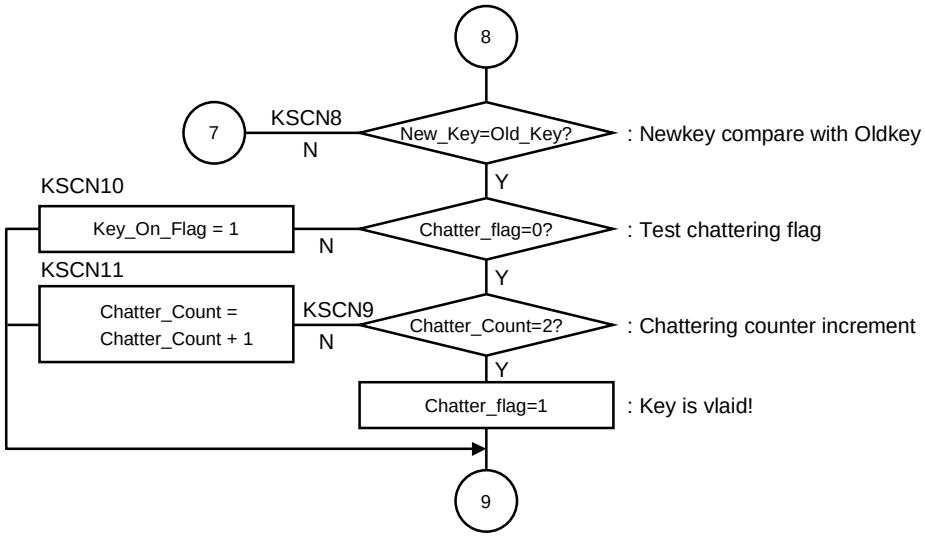
Name	Address	Description
CHATTER_COUNT	$00H	chatter counter -stores counter for couting number of key scan data comparison
KEY_NUMBER	$01H	stores key number
READ_DATA	$02H	stores depressed key data
NEW_KEY	$03H	stores current key data input
OLD_KEY	$04H	stores previous key data input
TOTAL_KEY	$05H	stores total number of pressed keys in the present key scan
R1_STROBE	$06H	stores strobe data
KEY_DATA	$07H	stores key number defined by key scan
KEY_FLAG	0, $08H	stores flag for indicating whether chatter elimination has been completed or not. if CHTCNT > 2, it is set to 1.
KEY_ON_FLAG	1, $08H	flag indicating whether key data is valid or not.

1-7. Flow Chart

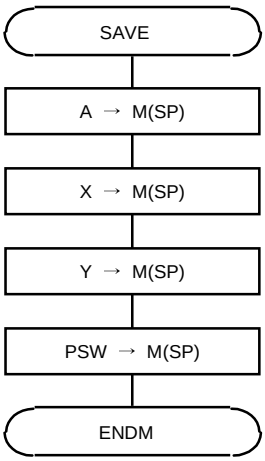



KSCAN
SAVE
: Reg. Save
9
KSCN7
Key_On_Flag=1?
: Test if key is processed
Y
N
Key_number ← 1
Total_Key ← 1
New_Key ← 0
r1strobe ← 1111_1110
: Initialize RAM
4
KSCN0
r1 ← r1_Strobe
nop
Read_Data ← r0
: Read key data
1
KSCN1
KSCN2
Read_Data = FFh?
: If Read-Data=ffh, key is pressed
Y
N
X ← 8
: Initialize loop counter
KSCN3
Right Rotate
Read_Data
: Read the column data
7
Y
Carry =1?
N
Carry =1?
N
Y
New Key ← Key_Number
Key_Number
=Key_Number
X ← X-1
: If carry = 1, next column read
Until X=0
N
X=0?
Y
5
KSCN5
: 1line check end

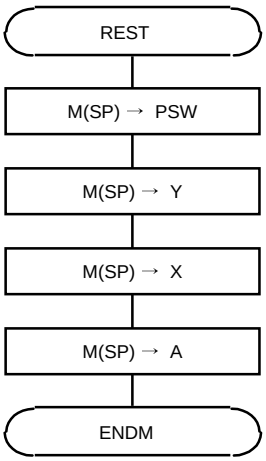

1
Key_Number
= 8+Key_Number
5
r1 ← $ffh
carry ← 1
r01 strobe
: Test if all line scan is completed
4
Y
Carry = 1?
N
8
N
New_Key=0?
: If newkey=0, key is not pressed
Y
7
KSCN6
Old_Key ← New_Key
Chatter_flag ← 0
Chatter_Count ← 0
: Newkey Save lear chattering flag
RESTORE
: Reg. Store
9
RET1



MACRO Definition
Save reg. to stack



Restore stack to reg.



GMS8xxxx Cross Assembler V1.55, By HYNIX Semiconductor, Inc.1995/12/12 15:05:11 (PAGE 1)

```
1                       NOLIST
95                  ;*************************************************************************
96                  ;           KEY SCAN FOR 8*8 KEY MATRIX
97                  ;*************************************************************************
98                  ;*************************************************************************
99                  ;           RAM ALLOCATION AREA
100                 ;*************************************************************************
101                 CHATTER_COUNT EQU  000H      ;CHATTERING COUNTER
102                 KEY_NUMBER EQU     001H      ;STORE KEY NUMBER
103                 READ_DATA EQU      002H      ;READ DATA FROM PORT
104                 NEW_KEY  EQU       003H      ;STORE CURRENT KEY DATA
105                 OLD_KEY  EQU       004H      ;STORE PREVIOUS KEY DATA
106                 TOTAL_KEY EQU      005H      ;TOTAL NUMBER OF KEY PRESS
107                 R1_STROBE EQU      006H      ;R1 PORT STROBE DATA
108                 KEY_DATA EQU       007H      ;DEFINED KEY NO.OF KEYSCAN
109                 KEY_FLAG EQU       008H
110                 CHATTER_FLAG EQU   0,008H     ;CHATTER_COUNT > 2,SET TO 1
111                 ;INDICATE CHATTERING END
112                 KEY_ON_FLAG EQU    1,008H     ;IF KEY IS VALID ,SET TO 1
113                 ;*************************************************************************
114                 ;  INT VECTOR DEFINITION
115                 ;*************************************************************************
116                 ;
117                       ORG    0FFE6H
118                 ;
119 FFE6  C4C0            DW     UNUSE            ;BASIC INTERVAL TIMER
120 FFE8  C4C0            DW     UNUSE            ;WATCH DOG TIMER
121 FFEA  C4C0            DW     UNUSE            ;A/D CON.
122 FFEC  C4C0            DW     UNUSE            ;TIMER-3
123 FFEE  40C0            DW     KEY_SCAN         ;KEY_SCAN  TIMER-2
124 FFF0  C4C0            DW     UNUSE            ;TIMER-1
125 FFF2  C4C0            DW     UNUSE            ;TIMER-0
126 FFF4  C4C0            DW     UNUSE            ;INT 3
127 FFF6  C4C0            DW     UNUSE            ;INT 2
128 FFF8  C4C0            DW     UNUSE            ;INT 1
129 FFFA  C4C0            DW     UNUSE            ;KEY SCAN
130 FFFC  C4C0            DW     UNUSE
131 FFFE  00C0            DW     RESET
132                 ;*************************************************************************
133                 ;               MACRO DEFINITION AREA
134                 ;*************************************************************************
135                 SAVE  MACRO
136                       PUSH   A
137                       PUSH   X
138                       PUSH   Y
139                       PUSH   PSW
```

GMS8xxxx Cross Assembler V1.55, By HYNIX Semiconductor, Inc.1995/12/12 15:05:11 (PAGE 2)

```
140                     ENDM
141
142             RESTORE MACRO
143                     POP   PSW
144                     POP   Y
145                     POP   X
146                     POP   A
147                     ENDM
148             ;*************************************************************************
149             ;           MAIN PROGRAM
150             ;*************************************************************************
151             ORG   0C000H
152             ;
153             ;-------------- RAM CLEAR, PORT INITIALIZE AND STOP ----------------------
154             ;
155 C000  C400  RESET:      LDA         #0
156 C002  1E00              LDX         #0
157 C004  FB    RAM_CLEAR: STA          {X}+
158 C005  5EC0              CMPX        #0C0H
159 C007  70FB              BNE         RAM_CLEAR
160 C009  1EFE              LDX         #0FEH
161 C00B  8E                TXSP                                ;STACK POINTER START
162             ; POSITION
163 C00C  60    RESTART:    DI
164 C00D  E4FFDE            LDM   R1ODC,#1111_1111B     ;R1 AS OPEN DRAIN
165 C010  E4FFC3            LDM   R1DD, #1111_1111B     ;OUTPUT PORT
166 C013  E482CE            LDM   IENH, #1000_0010B     ;KSCN,TIMER2 ENABLE
167 C016  E400CC            LDM   IENL, #0000_0000B     ;OTHER INT OFF
168 C019  E4FFDC            LDM   SMRR0, #1111_1111B    ;KEY SCAN RELEASE
169                                                     ;BY R00 ~ 07
170 C01C  E41DC7            LDM   CLKCTR,#0001_1101B    ;WDT_OFF, ENPCK_ON,16MS
171 C01F  E400C2            LDM   R1, #0000_0000B       ;R10 ~ R15 R1_STROBE ENABLE
172 C022  E405D2            LDM   TM2, #0000_0101B
173 C025  E427D9            LDM   T2DR, #39             ;39COUNT
174 C028  E41DD2            LDM   TM2, #0001_1101B      ;KEY SCAN,39*256=9.98mS
175 C02B  F1CF              CLR1   IRQKSCN
176 C02D  00                STOP
177 C02E  FF                NOP                         ;NEXT INSTRUCTION PATCH
178 C02F  FF                NOP                         ;WHEN EXECUTE STOP INST.
179
180 C030  E4FFC2            LDM    R1,#0FFH             ;R1(R1_STROBE)PORT ALL HIGH
181 C033  E0                EI
182 C034  3308FD  KEY_LOOP: BBC    KEY_ON_FLAG,$        ;IF VALID KEY IS DETECTED,
183 C037  60                DI                          ;INT.DISABLE AND GO TO
184 C038  3108              CLR1       KEY_ON_FLAG      ;RESTART
185 C03A  C503              LDA        NEW_KEY
```

GMS8xxxx Cross Assembler V1.55, By HYNIX Semiconductor, Inc.1995/12/12 15:05:11 (PAGE 3)

```
186 C03C   E507              STA     KEY_DATA              ;SAVE TO KEY_DATA
187 C03E   2FCC              BRA     RESTART               ;
188                ;
189                ;*************************************************************************
190                ;           KEY SCAN INT ROUTINE :TIMER 2
191                ;*************************************************************************
192                ;
193                KEY_SCAN: SAVE
194 C040   0E    @           PUSH  A
195 C041   2E    @           PUSH  X
196 C042   4E    @           USH   Y
197 C043   6E    @           PUSH  PSW
198 C044   23085D            BBS   KEY_ON_FLAG,KSCN7  ;TEST IF KEYDATA PROCESSED
199 C047   E40101            LDM   KEY_NUMBER,#1      ;RAM INITIALIZE
200 C04A   E40005            LDM   TOTAL_KEY,#0       ;
201 C04D   E40003            LDM   NEW_KEY,#0         ;
202 C050   E4FE06            LDM   R1_STROBE,#0FEH    ;FIRST STROBE (R10)
203 C053   C506  KSCN0:      LDA   R1_STROBE
204 C055   E5C2              STA   R1                 ;R1_STROBE -> R1 PORT
205 C057   FF                NOP
206 C058   FF                NOP
207 C059   C5C0              LDA   R0                 ;READ R0 PORT
208 C05B   FF                NOP
209 C05C   E502              STA   READ_DATA          ;DATA SAVE -> READ_DATA
210 C05E   44FF              CMP   #0FFH              ;KEY PRESSED?
211 C060   7009              BNE   KSCN2              ;KEY PRESSED
212 C062   20      KSCN1:    CLRC                     ;NO KEY PRESSED
213 C063   C408              LDA   #8
214 C065   0501              ADC   KEY_NUMBER
215 C067   E501              STA   KEY_NUMBER  ;      KEY_NUMBER=KEY_NUMBER+8
216 C069   2F1A              BRA   KSCN5
217 C06B   1E08   KSCN2:     LDX   #8                 ;ROTATE COUNT 8 TIME
218 C06D   6902   KSCN3:     ROR   READ_DATA
219 C06F   D00C              BCS   KSCN4              ;IF CARRY=1 -> KSCN4
220 C071   8905              INC   TOTAL_KEY          ;TOTAL_KEY=TOTAL_KEY+1
221 C073   C505              LDA   TOTAL_KEY
222 C075   4402              CMP   #2
223 C077   F024              BEQ   KSCN6              ;DOUBLE KEY PRESSED->KSCN6
224 C079   C501              LDA   KEY_NUMBER         ;KEY_NUMBER -> NEW_KEY
225 C07B   E503              STA   NEW_KEY
226 C07D   20      KSCN4:    CLRC
227 C07E   8901              INC   KEY_NUMBER
228 C080   AF                DEC   X                  ;COUNTER DECREMENT
229 C081   5E00              CMPX  #0
230 C083   70E8              BNE   KSCN3              ;COLUMN SCAN IS NOT END
231 C085   C4FF   KSCN5:     LDA   #0FFH              ;ONE LINE SCAN END
```

GMS8xxxx Cross Assembler V1.55, By HYNIX Semiconductor, Inc.1995/12/12 15:05:11 (PAGE 4)

```
232 C087   E5C2              STA    R1                        ;R1 PORT SET TO HIGH
233 C089   3BC6C0            CALL   !DELAY                    ;DELAY SOME TIME
234 C08C   A0                SETC
235 C08D   2906              ROL    R1_STROBE  ;NEXT LINE STROBE SAVE
236 C08F   C506              LDA    R1_STROBE  ;TO R1_STROBE
237 C091   44FF              CMP    #0FFH                     ;LINE SCAN FINISH?
238 C093   70BE              BNE    KSCN0                     ;NO -> KSCN0
239 C095   C503              LDA    NEW_KEY    ;LINE SCAN FINISH
240 C097   4400              CMP    #0                        ;IF NOKEY,NEW_KEY=0
241 C099   700E              BNE    KSCN8                     ;IF KEY PRESSED->KSCN8
242 C09B   C503              LDA    NEW_KEY    ;CLEAR FLAG,RAM
243 C09D   E504    KSCN6:    STA    OLD_KEY
244 C09F   1108              CLR1   CHATTER_FLAG
245 C0A1   E40000            LDM    CHATTER_COUNT,#0
246          KSCN7: RESTORE
247 C0A4   6D   @            POP    PSW
248 C0A5   4D   @            POP    Y
249 C0A6   2D   @            POP    X
250 C0A7   0D   @            POP    A
251 C0A8   7F                RETI
252 C0A9   C503    KSCN8:    LDA    NEW_KEY          ;NEW_KEY COMPARE WITH OLD_KEY
253 C0AB   4504              CMP    OLD_KEY
254 C0AD   70EE              BNE    KSCN6                     ;NOT SAME -> KSCN6
255 C0AF   03080A            BBS    CHATTER_FLAG,KSCN10;SAME,CHAT FLAG=1->KSCN10
256 C0B2   C500    KSCN9:    LDA    CHATTER_COUNT             ;IF CHAT FLAG=0,COMPARE
257 C0B4   4402              CMP    #2                        ;2TIME CHECK
258 C0B6   7008              BNE    KSCN11                    ;
259 C0B8   0108              SET1   CHATTER_FLAG              ;VALID KEY DATA
260 C0BA   2FE8              BRA    KSCN7
261 C0BC   2108    KSCN10:   SET1   KEY_ON_FLAG
262 C0BE   2FE4              BRA    KSCN7
263 C0C0   8900    KSCN11:   INC    CHATTER_COUNT             ;CHATTER_COUNT INCREMENT
264 C0C2   2FE0              BRA    KSCN7
265
266 C0C4   FF      UNUSE:    NOP
267 C0C5   7F                RETI
268 C0C6   FF      DELAY:    NOP
269 C0C7   FF                NOP
270 C0C8   6F                RET
271          ;
272                           NOLIST
```

-- 0 Error(s) --

--- Total Machine Code : 227 Bytes --

2. OUTPUT OF REMOCON SIGNAL

2-1. uPD6121G

2-1-1. Overview

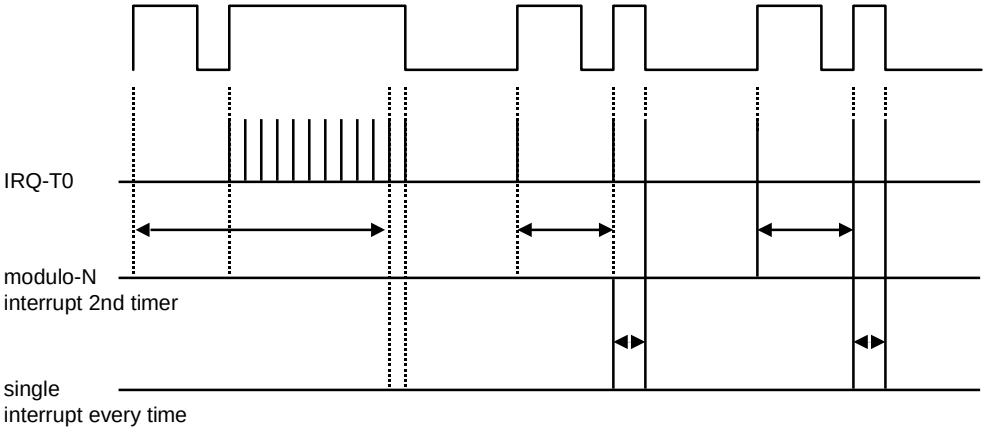
1) This program is example for uPD6121G
2) If shows the method of making carrier waveform by using Timer0 and Timer1
3) Waveform is generated by single mode and modulo-N combination

2-1-2. RAM Description

Label	Address	Description
CUSTOM	$00h	Store Custom Code
CUSTOM BAR	$01h	Complemented Custom Code
DATA	$02h	Store Data Code
DATA BAR	$03h	Complemented Data Code

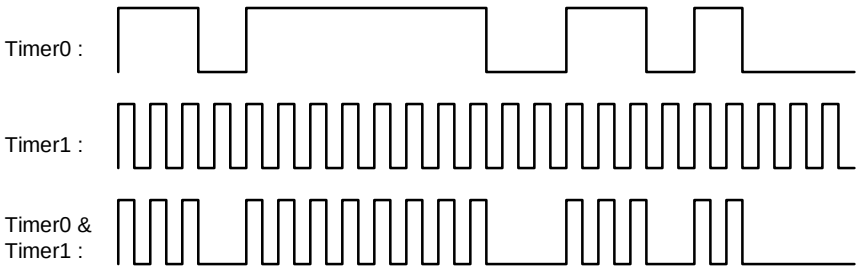
X reg = Byte Counter
Y reg = Bit Counter

2-1-3. Request flag & Timer setting



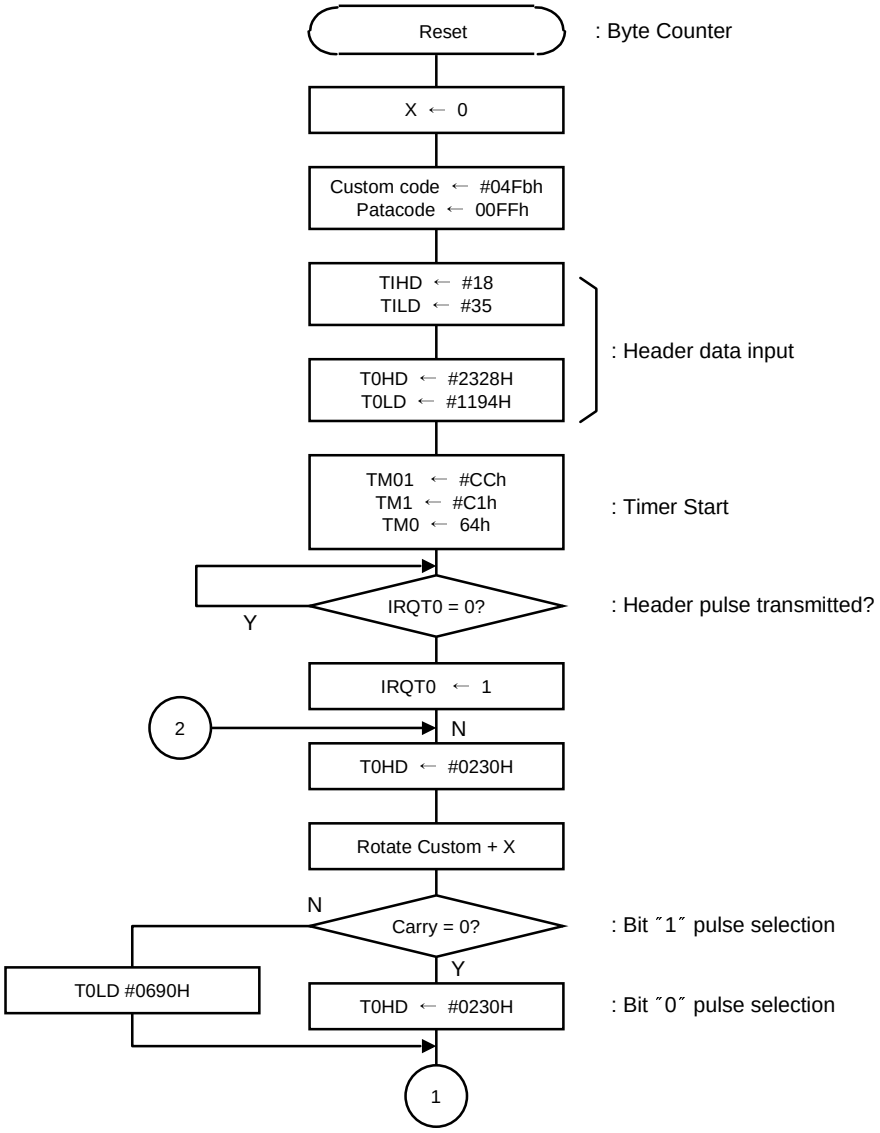
2-1-4. Module explanation

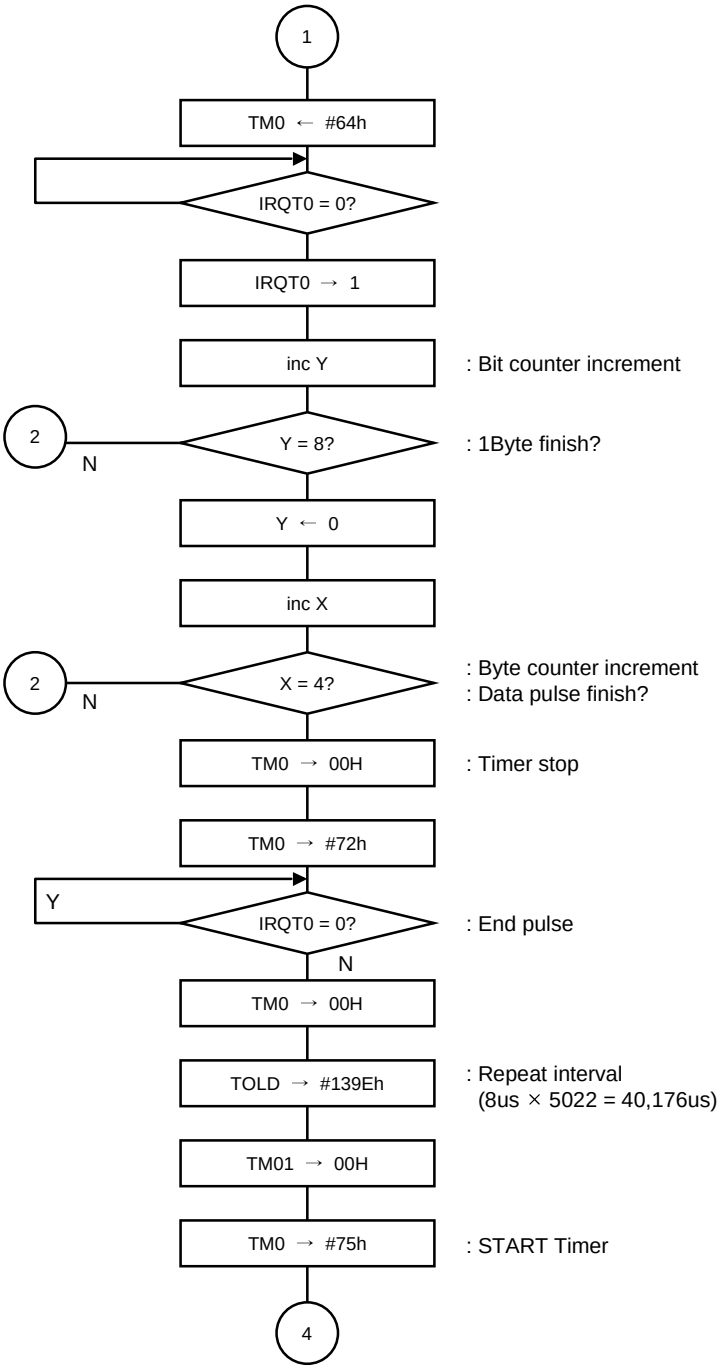
1) Timer0 is used to generate Remote output signal
2) Timer1 makes carrier frequency

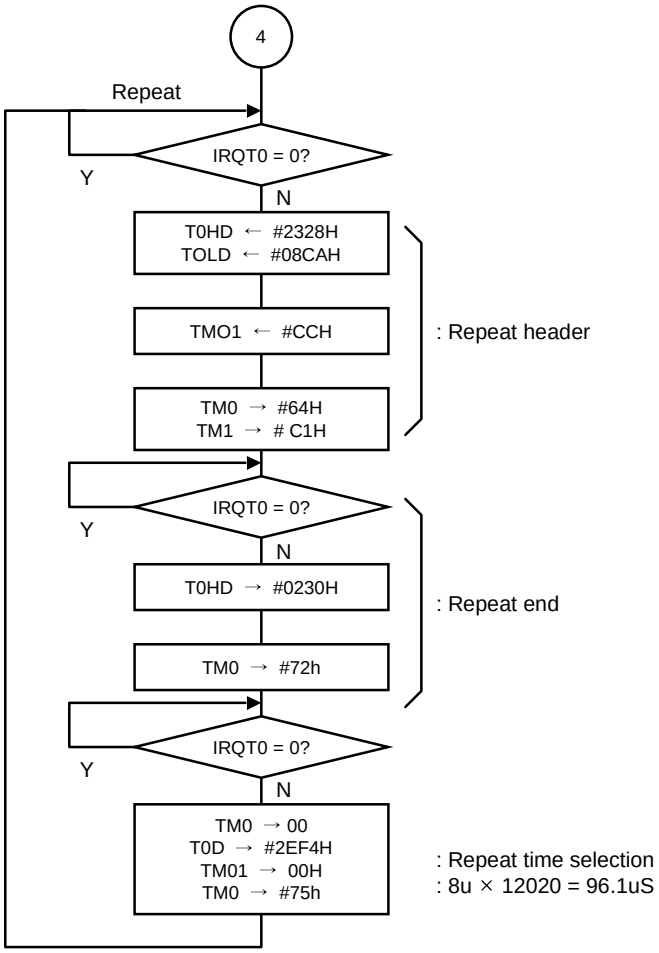


3) The Timer0 is changed from two interrupt to every interrupt before endpulse transmitt
4) Interrupt Request flag is used to know the timer count overflow

2-1-5. Flow Chart




1
TM0 ← #64h
IRQT0 = 0?
IRQT0 → 1
inc Y
: Bit counter increment
2
Y = 8?
N
: 1Byte finish?
Y ← 0
inc X
2
X = 4?
N
: Byte counter increment
: Data pulse finish?
TM0 → 00H
: Timer stop
TM0 → #72h
Y
IRQT0 = 0?
: End pulse
N
TM0 → 00H
TOLD → #139Eh
: Repeat interval
(8us × 5022 = 40,176us)
TM01 → 00H
TM0 → #75h
: START Timer
4


4
Repeat
IRQT0 = 0?
Y
N
T0HD ← #2328H
TOLD ← #08CAH
TMO1 ← #CCH
: Repeat header
TM0 → #64H
TM1 → # C1H
IRQT0 = 0?
Y
N
T0HD → #0230H
: Repeat end
TM0 → #72h
IRQT0 = 0?
Y
N
TM0 → 00
T0D → #2EF4H
TM01 → 00H
TM0 → #75h
: Repeat time selection
: 8u × 12020 = 96.1uS

GMS8xxxx Cross Assembler V1.55, By HYNIX Semiconductor, Inc.1995/12/12 15:00:04 (PAGE 1)

```
1                NOLIST
95               ;*************************************************************************
96               ;
97               ;                WAVE FORMAT FOR uPD6121G
98               ;
99               ;*************************************************************************
100              ;*************************************************************************
101              ;                RAM ALLOCATION AREA
102              ;*************************************************************************
103              ;*************************************************************************
104              ;                DATA RAM DEFINITION    (00H-0FH)
105              ;*************************************************************************
106              CUSTOM       EQU    000H                ;CUSTOM CODE
107              CUSTOM_BAR EQU    001H                ;CUSTOM_BAR CODE
108              DATA         EQU    002H                ;DATA CODE
109              DATA_BAR EQU      003H                ;DATA_BAR CODE
110
111              ;*************************************************************************;
112              ;                 INT VECTOR DEFINITION
113              ;*************************************************************************
114              ;
115                               ORG    0FFE6H
116              ;
117 FFE6  F4C0               DW     UNUSE               ; BASIC INTERVAL TIMER
118 FFE8  F4C0               DW     UNUSE               ; WATCH DOG TIMER
119 FFEA  F4C0               DW     UNUSE               ; A/D CON.
120 FFEC  F4C0               DW     UNUSE               ; TIMER-3
121 FFEE  F4C0               DW     UNUSE               ; TIMER-2
122 FFF0  F4C0               DW     UNUSE               ; TIMER-1
123 FFF2  F4C0               DW     UNUSE               ; TIMER-0
124 FFF4  F4C0               DW     UNUSE               ; INT 3
125 FFF6  F4C0               DW     UNUSE               ; INT 2
126 FFF8  F4C0               DW     UNUSE               ; INT 1
127 FFFA  F4C0               DW     UNUSE               ; KEY SCAN
128 FFFC  F4C0               DW     UNUSE
129 FFFE  00C0               DW     RESET
130
131              ;*************************************************************************
132              ;                MACRO DEFINITION
133              ;*************************************************************************
134                 SAVE         MACRO
135                               PUSH   A
136                               PUSH   X
137                               PUSH   Y
138                               PUSH   PSW
139                               ENDM
```

```
140
141                     RESTORE  MACRO
142                      POP    PSW
143                      POP    Y
144                      POP    X
145                      POP    A
146                      ENDM
147                     ;*********************************************************************
148                     ;            MAIN PROGRAM
149                     ;*********************************************************************
150                     ORG    0C000H
151 C000  C400    RESET:        LDA    #0
152 C002  1E00                  LDX    #0                      ; RAM CLEAR
153 C004  FB        RAMCLR:     STA    {X}+
154 C005  5EC0                  CMPX   #0C0H
155 C007  70FB                  BNE    RAMCLR
156 C009  1EFE                  LDX    #0FEH
157 C00B  8E                    TXSP                           ; STACK POINTER INITIALIZE
158 C00C  60                    DI
159 C00D  E4FFDE                LDM    R1ODC,#1111_1111B   ; R1 AS OPEN DRAIN
160 C010  E4FFC3                LDM    R1DD,#1111_1111B  ; OUTPUT PORT
161 C013  E4FFC2                LDM    R1,#1111_1111B
162 C016  E480CE                LDM    IENH,#1000_0000B   ; KSCN ENABLE
163 C019  E41FC5                LDM    R2DD,#0001_1111B  ;
164 C01C  E41FC4                LDM    R2,#0001_1111B         ; R2 AS OUTPUT
165 C01F  E4FFDC                LDM    SMRR0,#1111_1111B  ; KEY SCAN RELEASE
166                                                            ; BY R00~07
167 C022  E41DC7                LDM    CLKCTR,#0001_1101B   ; WDT_OFF, ENPCK_OFF, 16MS(PS8)
168 C025  E400C2                LDM    R1,#00H                ; R10 ~ R15 STROBE ENABLE
169 C028  F1CF                  CLR1   IRQKSCN
170 C02A  00                    STOP
171 C02B  FF                    NOP
172 C02C  E4FFC2                LDM    R1,#1111_1111B
173                     ;               CALL    KEY_SCAN
174
175
176                     ;*********************************************************************
177                     ;            TRANSMITTING KEY DATA
178                     ;*********************************************************************
179 C02F  1E00      NEC_MODE: LDX     #00H
180 C031  3E00                  LDY    #00H
181 C033  E40400                LDM    CUSTOM,#04H   ;CUSTOM CODE:04FBH
182 C036  E4FB01                LDM    CUSTOM_BAR,#0FBH
183 C039  E40002                LDM    DATA,#00H    ;DATA CODE:00FFH
184 C03C  E4FF03                LDM    DATA_BAR,#0FFH
185 C03F  E400D0                LDM    TM0,#00H
```

GMS8xxxx Cross Assembler V1.55, By HYNIX Semiconductor, Inc.1995/12/12 15:00:04 (PAGE 3)

```
186 C042  E412D7                LDM    T1HD,#18              ;CARRIER FRE=0.5uS*18=9.0uS
187 C045  E423D8                LDM    T1LD,#35              ;0.5uS*35=17.5uS
188 C048  E423D3                LDM    T0HMD,#23H            ;9MS PER 1US
189 C04B  E428D4                LDM    T0HLD,#28H
190 C04E  E411D5                LDM    T0LMD,#11H            ;4.5MS PER 1US
191 C051  E494D6                LDM    T0LLD,#94H
192 C054  E4CCDA                LDM    TM01,#1100_1100B  ;T0 & T1 OUTPUT
193 C057  E4C1D1                LDM    TM1,#1100_0001B       ;MODULO_EVERY_500nS
194 C05A  E46AD0                LDM    TM0,#0110_1010B       ;MODULO_SECOND_1uS
195 C05D  73CFFD                BBC    IRQT0,$               ;WAIT UNTIL MATCH THE TIME
196 C060  4BCF60                NOT1   IRQT0                 ;
197 C063  E402D3  PUL_START: LDM    T0HMD,#02H            ;560US
198 C066  E430D4                LDM    T0HLD,#30H
199 C069  7900                  ROR    CUSTOM+X
200 C06B  5008                  BCC    LOW_OUT
201
202 C06D  E406D5  HIGH_OUT: LDM T0LMD,#06H             ;1680US
203 C070  E490D6                LDM    T0LLD,#90H
204 C073  2F08                  BRA    PUL_TEST
205 C075  E402D5  LOW_OUT: LDM  T0LMD,#02H             ;560US
206 C078  E430D6                LDM    T0LLD,#30H
207 C07B  2F00                  BRA    PUL_TEST
208
209 C07D  E46AD0  PUL_TEST: LDM   TM0,#0110_1010B ;TIMER0 START
210 C080  73CFFD                BBC    IRQT0,$               ;BIT OUT
211 C083  4BCF60                NOT1   IRQT0
212 C086  9E                    INC    Y
213 C087  7E08                  CMPY   #8                    ;IF BIT_COUNTER =8 ,
214 C089  70D8                  BNE    PUL_START             ;1 BYTE PULSE OUT
215 C08B  3E00                  LDY    #0                    ;BIT_COUNTER CLEAR
216 C08D  8F                    INC    X                     ;BYTE COUNTER X INC
217 C08E  5E04                  CMPX   #4
218 C090  70D1                  BNE    PUL_START
219                     ;DATA PULSE OUT FINISH
220 C092  E400D0                LDM    TM0,#00H
221 C095  E472D0                LDM    TM0,#0111_0010B   ;TIM,STA,CONT,SING,EVE,1US
222 C098  73CFFD                BBC    IRQT0,$               ;END PULSE OUT
223 C09B  4BCF60                NOT1   IRQT0
224 C09E  E400D0                LDM    TM0,#00H
225 C0A1  E413D5                LDM    T0LMD,#13H            ;REPEAT TIME SET
226 C0A4  E49ED6                LDM    T0LLD,#9EH            ; (8US*5022=40.176MS)
227 C0A7  E400DA                LDM    TM01,#00H
228 C0AA  E475D0                LDM    TM0,#0111_0101B  ;TIM,STA,CONT,SING,EVE,8US
229
230                     ;-------------- REPEAT PULSE OUT ----------------------------------------
231 C0AD  73CFFD  REPEAT:  BBC    IRQT0,$               ;WAITING FOR 40.176MS
```

GMS8xxxx Cross Assembler V1.55, By HYNIX Semiconductor, Inc.1995/12/12 15:00:04 (PAGE 4)

```
232 C0B0   4BCF60          NOT1   IRQT0
233 C0B3   E400D0          LDM    TM0,#00H
234 C0B6   E423D3          LDM    T0HMD,#23H   ;9MS PER 1US
235 C0B9   E428D4          LDM    T0HLD,#28H
236 C0BC   E408D5          LDM    T0LMD,#08H   ;2.25MS PER 1US
237 C0BF   E4CAD6          LDM    T0LLD,#0CAH
238 C0C2   E4CCDA          LDM    TM01,#1100_1100B   ;T0 & T1 OUTPUT
239 C0C5   E46AD0          LDM    TM0,#0110_1010B   ;MODULO_SECOND_1uS
240 C0C8   E4C1D1          LDM    TM1,#1100_0001B   ;MODULO_EVERY_500nS
241 C0CB   73CFFD          BBC    IRQT0,$
242 C0CE   4BCF60          NOT1   IRQT0
243 C0D1   E400D0          LDM    TM0,#00H
244 C0D4   E402D3          LDM    T0HMD,#02H   ;560US
245 C0D7   E430D4          LDM    T0HLD,#30H
246 C0DA   E472D0          LDM    TM0,#0111_0010B   ;END PULSE OUT
247 C0DD   73CFFD          BBC    IRQT0,$
248 C0E0   4BCF60          NOT1   IRQT0
249 C0E3   E400D0          LDM    TM0,#00H    ;
250 C0E6   E42ED5          LDM    T0LMD,#2EH   ;REPEAT TIME SET
251 C0E9   E4F4D6          LDM    T0LLD,#0F4H   ;(8US*12020=96.16MS)
252 C0EC   E400DA          LDM    TM01,#00H
253 C0EF   E475D0          LDM    TM0,#0111_0101B   ;TIM,STA,CONT,SING,EVE,8US
254 C0F2   2FB9            BRA    REPEAT      ;TIMER0 START WHILE REPEAT
255
256 C0F4   FF      UNUSE:  NOP
257 C0F5   7F              RETI
258                        END
```

-- 0 Error(s) --

--- Total Machine Code : 272 Bytes --

2-2. TC9012

2-2-1. Overview

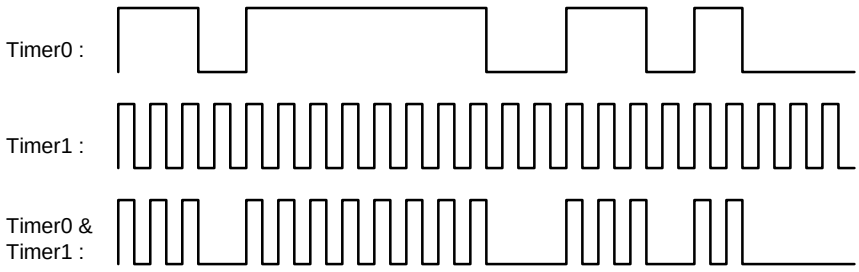
1) This program is example for TC9012
2) If shows the method of making carrier waveform by using Timer0 and Timer1
3) Waveform is generated by single mode and modulo-N combination

2-1-2. RAM Description

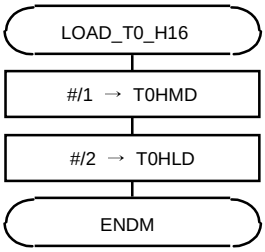
Label	Address	Description
NEWKEY	$03H	Valid Key Data Come From Key Scan Routine
KEYDATA	$07H	OLD Key Data
REPEAT	2, $08H	Repeat Flag
COUNT	$0AH	Bit Count
BUFFER	$0BH	Custom Data
BUFFER1	$0CH	Custom Complemented Data
BUFFER2	$0DH	Key Data
BUFFER3	$0EH	Complemented Key Data

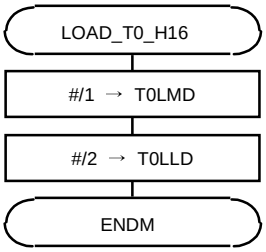
2-2-3. Module explanation

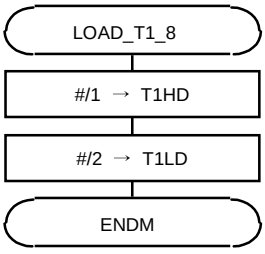
1) Timer0 is used to generate remote output signal
2) Timer1 makes carrier frequency
3) Timer0/1 : Modulo-N interrupt every counter overflow

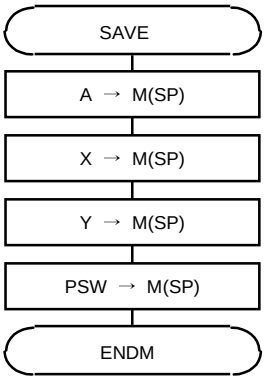


2-2-4. Flow Chart

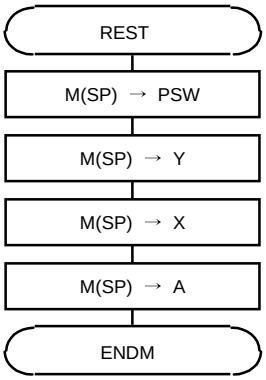




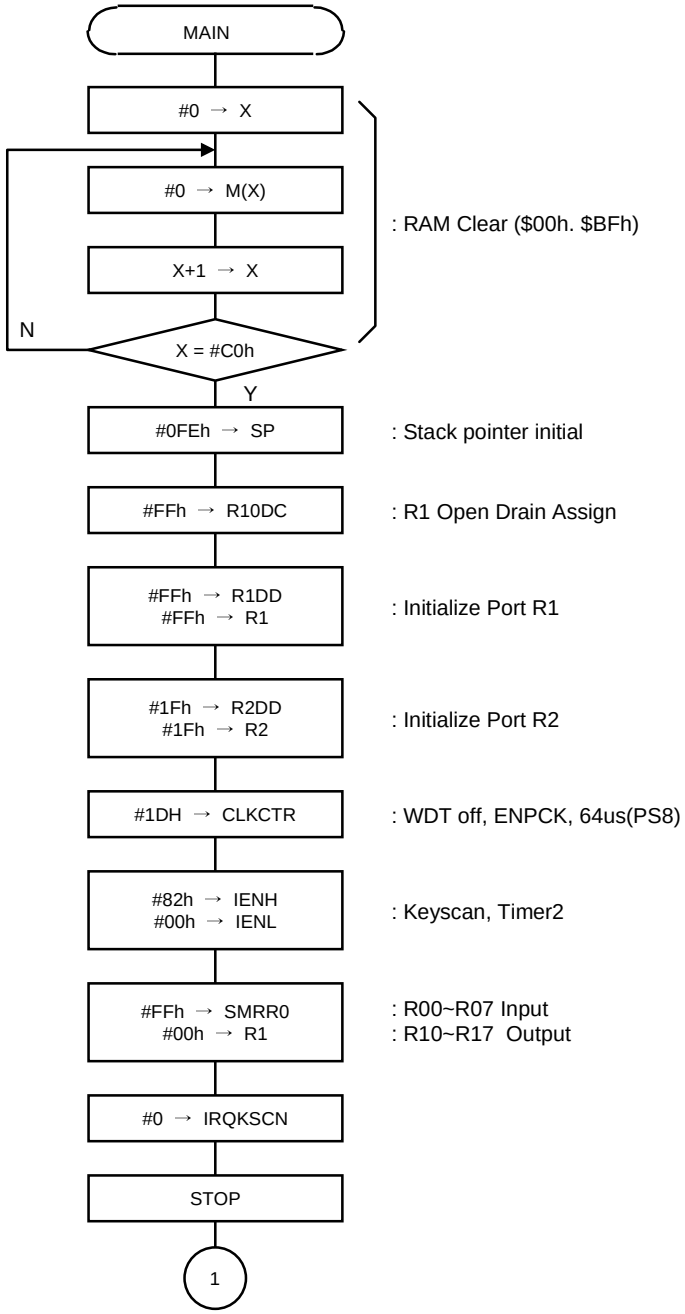


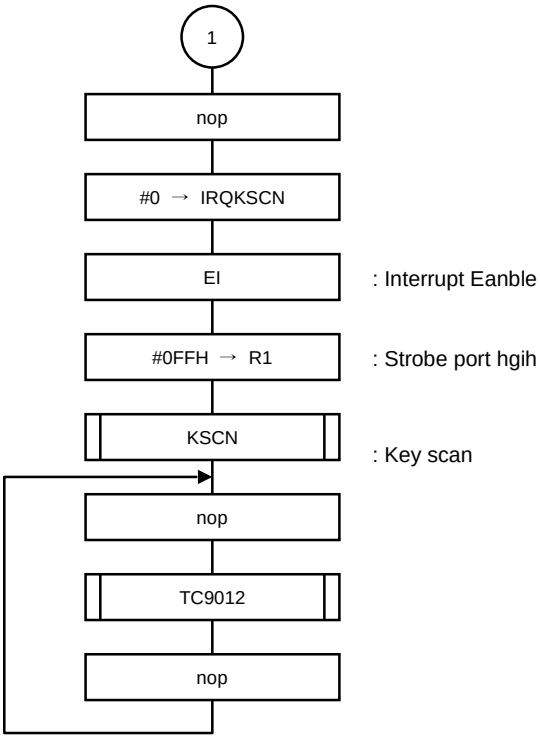


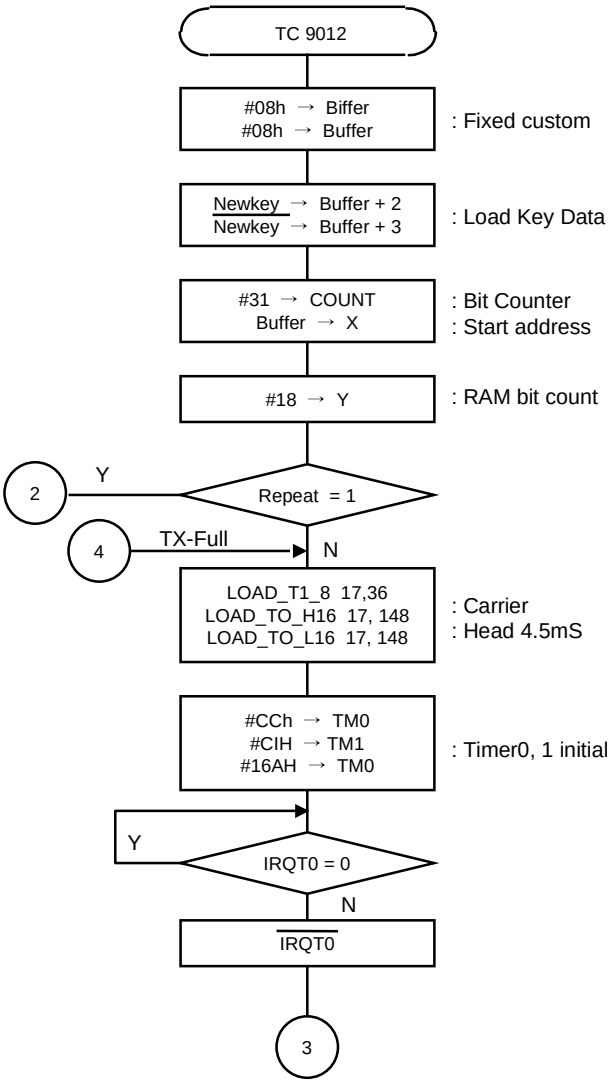
: Save reg. to stack

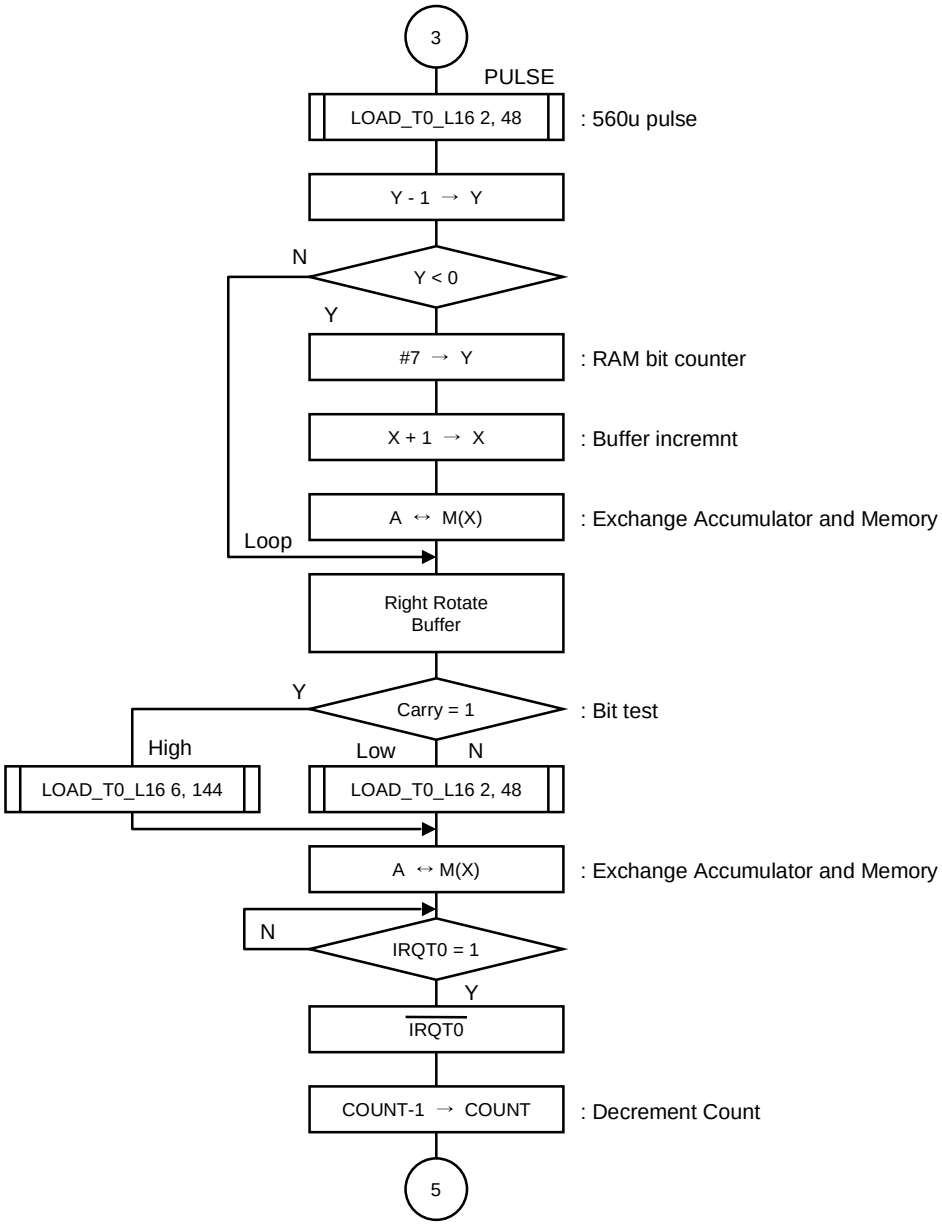


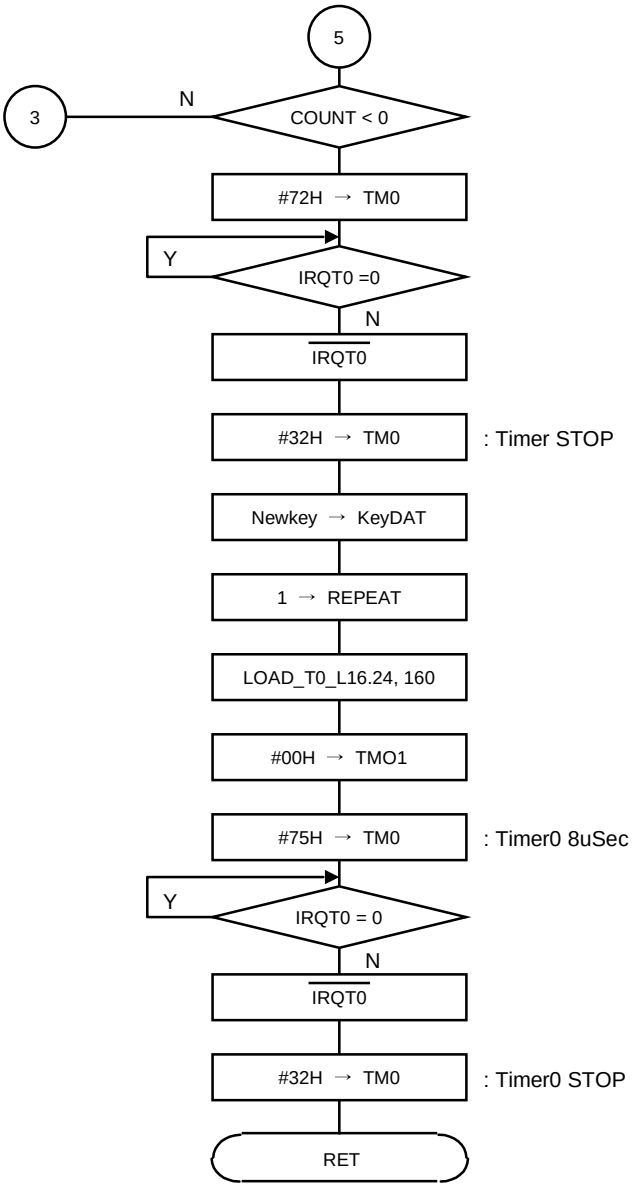
: Restore stack to reg.

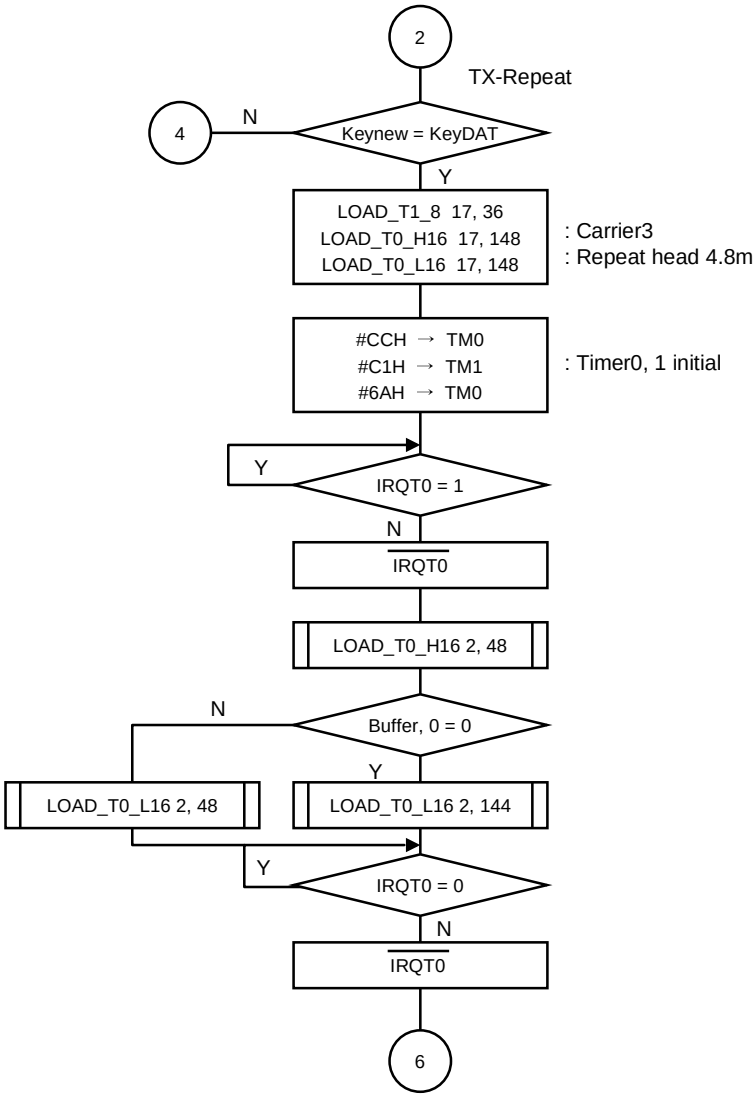

MAIN
#0 → X
#0 → M(X)
X+1 → X
N
X = #C0h
Y
#0FEh → SP
#FFh → R10DC
#FFh → R1DD
#FFh → R1
#1Fh → R2DD
#1Fh → R2
#1DH → CLKCTR
#82h → IENH
#00h → IENL
#FFh → SMRR0
#00h → R1
#0 → IRQKSCN
STOP
1
: RAM Clear ($00h. $BFh)
: Stack pointer initial
: R1 Open Drain Assign
: Initialize Port R1
: Initialize Port R2
: WDT off, ENPCK, 64us(PS8)
: Keyscan, Timer2
: R00~R07 Input
: R10~R17 Output

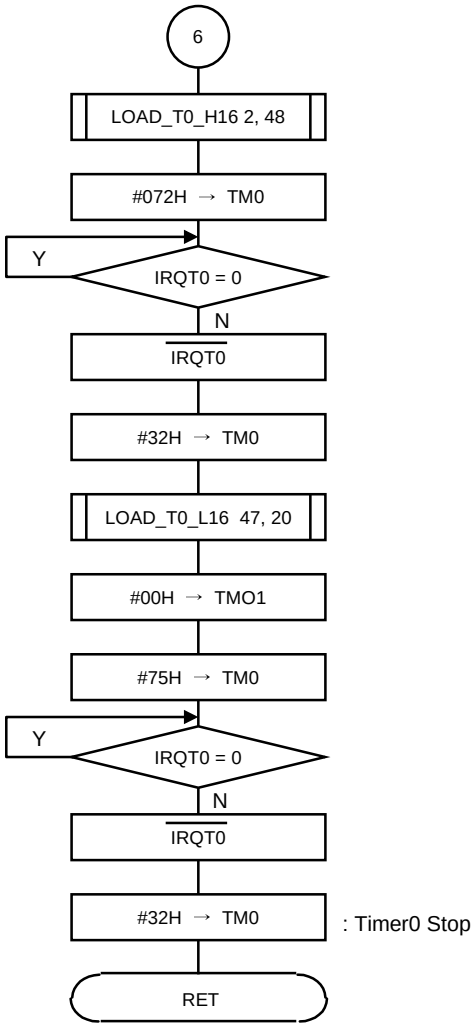

1
nop
#0 → IRQKSCN
EI
: Interrupt Eanble
#0FFH → R1
: Strobe port hgih
KSCN
: Key scan
nop
TC9012
nop


TC 9012
#08h → Biffer
#08h → Buffer
: Fixed custom
Newkey → Buffer + 2
Newkey → Buffer + 3
: Load Key Data
#31 → COUNT
Buffer → X
: Bit Counter
: Start address
#18 → Y
: RAM bit count
2
Y
Repeat = 1
4
TX-Full
N
LOAD_T1_8 17,36
LOAD_TO_H16 17, 148
LOAD_TO_L16 17, 148
: Carrier
: Head 4.5mS
#CCh → TM0
#CIH → TM1
#16AH → TM0
: Timer0, 1 initial
Y
IRQT0 = 0
N
IRQT0
3


3
PULSE
LOAD_T0_L16 2, 48
: 560u pulse
Y - 1 → Y
N
Y < 0
Y
#7 → Y
: RAM bit counter
X + 1 → X
: Buffer incremnt
A ↔ M(X)
: Exchange Accumulator and Memory
Loop
Right Rotate
Buffer
Y
Carry = 1
: Bit test
High
Low
N
LOAD_T0_L16 6, 144
LOAD_T0_L16 2, 48
A ↔ M(X)
: Exchange Accumulator and Memory
N
IRQT0 = 1
Y
IRQT0
COUNT-1 → COUNT
: Decrement Count
5


5
3
N
COUNT < 0
#72H → TM0
Y
IRQT0 =0
N
IRQT0
#32H → TM0
: Timer STOP
Newkey → KeyDAT
1 → REPEAT
LOAD_T0_L16.24, 160
#00H → TMO1
#75H → TM0
: Timer0 8uSec
Y
IRQT0 = 0
N
IRQT0
#32H → TM0
: Timer0 STOP
RET


2
TX-Repeat
4
N
Keynew = KeyDAT
Y
LOAD_T1_8 17, 36
LOAD_T0_H16 17, 148
LOAD_T0_L16 17, 148
: Carrier3
: Repeat head 4.8m
#CCH → TM0
#C1H → TM1
#6AH → TM0
: Timer0, 1 initial
Y
IRQT0 = 1
N
IRQT0
LOAD_T0_H16 2, 48
N
Buffer, 0 = 0
Y
LOAD_T0_L16 2, 48
LOAD_T0_L16 2, 144
Y
IRQT0 = 0
N
IRQT0
6


6
LOAD_T0_H16 2, 48
#072H → TM0
Y
IRQT0 = 0
N
IRQT0
#32H → TM0
LOAD_T0_L16 47, 20
#00H → TMO1
#75H → TM0
Y
IRQT0 = 0
N
IRQT0
#32H → TM0
: Timer0 Stop
RET

GMS8xxxx Cross Assembler V1.55, By HYNIX Semiconductor, Inc.1995/12/12 14:59:46 (PAGE 1)

```
1               NOLIST
95          ;=====================================================================
96          ;
97          ;           TC9012  TX  PROGRAM
98          ;
99          ;=====================================================================
100         ;=====================================================================
101         ;           RAM  ALLOCATION
102         ;=====================================================================
103         ;
104         NEWKEY   EQU    03H             ;NEW KEY NUMBER
105         KEYDAT   EQU    07H             ;OLD KEY DATA
106         REPEAT   EQU    2,08H           ;REPEAT FLAG
107         COUNT    EQU    0AH             ;BIT COUNT
108         BUFFER   EQU    0BH             ;CUSTOM TX DATA RAM
109         BUFFER1  EQU    0CH             ;CUSTOM_BAR TX DATA RAM
110         BUFFER2  EQU    0DH             ;KEY TX DATA RAM
111         BUFFER3  EQU    0EH             ;KEY DATA_BAR TX RAM
112         ;
113         ;=====================================================================
114         ;           MACRO  DEFINITION
115         ;=====================================================================
116         LOAD_T0_H16 MACRO               ;LOAD HIGH_DATA FOR TIMER0
117                     LDM    T0HMD,#\1
118                     LDM    T0HLD,#\2
119                     ENDM
120         ;
121         LOAD_T0_L16 MACRO               ;LOAD LOW_DATA FOR TIMER0
122                     LDM    T0LMD,#\1
123                     LDM    T0LLD,#\2
124                     ENDM
125         ;
126         LOAD_T1_8 MACRO                 ;LOAD 8BIT DATA FOR TIMER1
127                     LDM    T1HD,#\1
128                     LDM    T1LD,#\2
129                     ENDM
130         ;
131         SAVE    MACRO                   ;REGISTER SAVE
132                     PUSH   A
133                     PUSH   X
134                     PUSH   Y
135                     PUSH   PSW
136                     ENDM
137         ;
138         REST    MACRO                   ;REGISTER RESTORE
139                     POP    PSW
```

GMS8xxxx Cross Assembler V1.55, By HYNIX Semiconductor, Inc.1995/12/12 14:59:46 (PAGE 2)

```
140                                             POP    Y
141                                             POP    X
142                                             POP    A
143                                             ENDM
144             ;
145             ;===============================================================
146             ;           INTERRUPT  VECTOR  TABLE
147             ;===============================================================
148             ;
149                     ORG    0FFE4H
150         ;
151 FFE4  FF    NOTUSE:  NOP
152 FFE5  7F             RETI
153         ;
154 FFE6  E4FF           DW     NOTUSE          ;BASIC INTERVAL TIMER
155 FFE8  E4FF           DW     NOTUSE          ;WATCH DOG TIMER
156 FFEA  E4FF           DW     NOTUSE          ;A/D CONVERTER
157 FFEC  E4FF           DW     NOTUSE          ;TIMER-3
158 FFEE  E4FF           DW     NOTUSE          ;TIMER-2
159 FFF0  E4FF           DW     NOTUSE          ;TIMER-1
160 FFF2  E4FF           DW     NOTUSE          ;TIMER-0
161 FFF4  E4FF           DW     NOTUSE          ;INT 3
162 FFF6  E4FF           DW     NOTUSE          ;INT 2
163 FFF8  E4FF           DW     NOTUSE          ;INT 1
164 FFFA  E4FF           DW     NOTUSE          ;KEY SCAN
165 FFFC  E4FF           DW     NOTUSE
166 FFFE  00C0           DW     MAIN            ;RESET
167             ;
168             ;=====================================================================
169             ;           MAIN  PROGRAM
170             ;=====================================================================
171             ;
172                                             ORG    0C000H
173 C000  1E00   MAIN:   LDX    #0
174 C002  C400           LDA    #0              ;RAM CLEAR(!0000H->!00BFH)
175 C004  FB             CLR:                   STA    {X}+
176 C005  5EC0           CMPX   #0C0H
177 C007  70FB           BNE    CLR
178 C009  1EFE           LDX    #0FEH           ;STACK POINTER INITIAL
179 C00B  8E             TXSP
180         ;
181 C00C  E4FFDE         LDM    R1ODC,#0FFH     ;R1 OPEN DRAIN ASSIGN REG.
182 C00F  E4FFC3         LDM    R1DD,#0FFH      ;DATA DIRECTION REG.
183 C012  E4FFC2         LDM    R1,#0FFH        ;R1 DATA REG.
184 C015  E41FC5         LDM    R2DD,#1FH       ;DATA DIRECTION REG.
185 C018  E41FC4         LDM    R2,#1FH         ;R2 DATA REG. OUTPUT
```

GMS8xxxx Cross Assembler V1.55, By HYNIX Semiconductor, Inc.1995/12/12 14:59:46 (PAGE 3)

```
186 C01B   E41DC7              LDM    CLKCTR,#1DH   ;WDT OFF, ENPCK, 64uS(PS8)
187 C01E   E480CE              LDM    IENH,#80H     ;KEYSCAN
188 C021   E400CC              LDM    IENL,#00H     ;WATCH DOG TIMER
189 C024   E4FFDC              LDM    SMRR0,#0FFH   ;R00~7 INPUT
190 C027   E400C2              LDM    R1,#00H       ;R10~7 STROBE ENABLE(OUTPUT)
191 C02A   F1CF                CLR1   IRQKSCN
192 C02C   00                  STOP
193          ;
194 C02D   FF                  NOP
195 C02E   F1CF                CLR1   IRQKSCN
196 C030   E0                  EI
197 C031   E4FFC2              LDM    R1,#0FFH      ;STROBE PORT HIGH
198 C034   3B3BC1              CALL    KSCN         ;TEST IF KEY PRESSED
199 C037   FF          TX_LOOP: NOP
200 C038   3B3EC0              CALL   TC9012
201 C03B   FF                  NOP
202 C03C   2FF9                BRA    TX_LOOP
203                    ;
204                    ;================================================================
205                    ;            TC9012  TX  ROUTINE
206                    ;================================================================
207                    ;
208 C03E   E4080B     TC9012:  LDM    BUFFER,#08H   ;FIXED CUSTOM
209 C041   E4080C              LDM    BUFFER+1,#08H
210 C044   C503                LDA     NEWKEY
211 C046   E50D                STA     BUFFER+2
212 C048   E50E                STA    BUFFER+3
213 C04A   2C0E                COM     BUFFER+3      ;
214 C04C   E41F0A              LDM    COUNT,#31     ;BIT COUNT
215 C04F   1E0B                LDX     #BUFFER      ;START ADDRESS
216 C051   3E08                LDY     #8           ;RAM BIT COUNT
217 C053   430874              BBS     REPEAT,TX_REPEAT   ;REPEAT CHECK
218                    ;
219                    TX_FULL: LOAD_T1_8 17,36      ;CARRIER HI=500nS*17=8.5uS
220 C056   E411D7 @            LDM    T1HD,#17
221 C059   E424D8 @            LDM    T1LD,#36
222                    LOAD_T0_H16 17,148            ;4.5mS
223 C05C   E411D3 @            LDM    T0HMD,#17
224 C05F   E494D4 @            LDM    T0HLD,#148
225                    LOAD_T0_L16 17,148            ;4.5mS
226 C062   E411D5 @            LDM    T0LMD,#17
227 C065   E494D6 @            LDM    T0LLD,#148
228 C068   E4CCDA              LDM    TM01,#0CCH    ;T0/1 HIGH T0 AND T1
229 C06B   E4C1D1              LDM    TM1,#0C1H     ;500nS, MODULO
230 C06E   E46AD0              LDM    TM0,#06AH     ;1uS
231 C071   73CFFD              BBC    IRQT0,$       ;HEAD PULSE
```

GMS8xxxx Cross Assembler V1.55, By HYNIX Semiconductor, Inc.1995/12/12 14:59:46 (PAGE 4)

```
232 C074   4BCF60              NOT1   IRQT0
233                    ;
234                    PULSE: LOAD_T0_H16 2,48        ;560uS
235 C077   E402D3 @            LDM    T0HMD,#2
236 C07A   E430D4 @            LDM    T0HLD,#48
237 C07D   BE                  DEC    Y
238 C07E   1003                BPL    LOOP
239 C080   3E07                LDY    #7              ;RAM BIT COUNT
240 C082   8F                  INC    X               ;BUFFER INCREMENT
241 C083   BB                  LOOP:  XMA    {X}
242 C084   68                  ROR    A
243 C085   D008                BCS    HIGH
244                    LOAD_T0_L16 2,48               ;560uS
245 C087   E402D5 @            LDM    T0LMD,#2
246 C08A   E430D6 @            LDM    T0LLD,#48
247 C08D   2F06                BRA    LOW
248                    ;
249                    HIGH: LOAD_T0_L16 6,144        ;1.68mS
250 C08F   E406D5 @            LDM    T0LMD,#6
251 C092   E490D6 @            LDM    T0LLD,#144
252 C095   BB          LOW:    XMA    {X}
253 C096   73CFFD              BBC    IRQT0,$
254 C099   4BCF60              NOT1   IRQT0
255 C09C   A90A                DEC    COUNT
256 C09E   9002                BMI    TX_END          ;32BIT TX COMPLETE
257 C0A0   2FD5                BRA    PULSE
258          ;
259 C0A2   E472D0  TX_END:     LDM    TM0,#072H
260 C0A5   73CFFD              BBC    IRQT0,$
261 C0A8   4BCF60              NOT1   IRQT0
262 C0AB   E432D0              LDM    TM0,#32H        ;TIMER0 STOP
263 C0AE   C503                LDA    NEWKEY
264 C0B0   E507                STA    KEYDAT
265 C0B2   4108                SET1   REPEAT
266                    ;
267                    LOAD_T0_L16 24,160
268 C0B4   E418D5 @            LDM    T0LMD,#24
269 C0B7   E4A0D6 @            LDM    T0LLD,#160
270 C0BA   E400DA              LDM    TM01,#00H
271 C0BD   E475D0              LDM    TM0,#75H        ;COUNT, PS5(8uS)
272 C0C0   73CFFD              BBC    IRQT0,$
273 C0C3   4BCF60              NOT1   IRQT0
274 C0C6   E432D0              LDM    TM0,#32H        ;TIMER0 STOP
275 C0C9   6F                  RET
276                    ;
277                    ;==================    REPEAT ROUTINE  ====================
```

GMS8xxxx Cross Assembler V1.55, By HYNIX Semiconductor, Inc.1995/12/12 14:59:46 (PAGE 5)

```
278           ;
279 C0CA  C503        TX_REPEAT:  LDA    NEWKEY
280 C0CC  4507                    CMP    KEYDAT
281 C0CE  7086                    BNE    TX_FULL
282                   LOAD_T1_8 17,36                  ;CARRIER HI=500nS*17=8.5uS
283 C0D0  E411D7 @                LDM    T1HD,#17
284 C0D3  E424D8 @                LDM    T1LD,#36
285                   LOAD_T0_H16 17,148               ;4.5mS
286 C0D6  E411D3 @                LDM    T0HMD,#17
287 C0D9  E494D4 @                LDM    T0HLD,#148
288                   LOAD_T0_L16 17,148               ;4.5mS
289 C0DC  E411D5 @                LDM    T0LMD,#17
290 C0DF  E494D6 @                LDM    T0LLD,#148
291 C0E2  E4CCDA                  LDM    TM01,#0CCH    ;T0/1 HIGH T0 AND T1
292 C0E5  E4C1D1                  LDM    TM1,#0C1H     ;500nS, MODULO
293 C0E8  E46AD0                  LDM    TM0,#06AH     ;1uS
294 C0EB  73CFFD                  BBC    IRQT0,$       ;HEAD PULSE
295 C0EE  4BCF60                  NOT1   IRQT0
296                   ;
297                   LOAD_T0_H16 2,48                 ;560uS
298 C0F1  E402D3 @                LDM    T0HMD,#2
299 C0F4  E430D4 @                LDM    T0HLD,#48
300 C0F7  130B08                  BBC    BUFFER.0,TH
301                   LOAD_T0_L16 2,48                 ;560uS
302 C0FA  E402D5 @                LDM    T0LMD,#2
303 C0FD  E430D6 @                LDM    T0LLD,#48
304 C100  2F06                    BRA    TL
305                   TH: LOAD_T0_L16 6,144            ;1.68mS
306 C102  E406D5 @                LDM    T0LMD,#6
307 C105  E490D6 @                LDM    T0LLD,#144
308 C108  73CFFD  TL:             BBC    IRQT0,$
309 C10B  4BCF60                  NOT1   IRQT0
310                   ;
311                   LOAD_T0_H16 2,48                 ;560uS
312 C10E  E402D3 @                LDM    T0HMD,#2
313 C111  E430D4 @                LDM    T0HLD,#48
314 C114  E472D0                  LDM    TM0,#072H
315 C117  73CFFD                  BBC    IRQT0,$
316 C11A  4BCF60                  NOT1   IRQT0
317 C11D  E432D0                  LDM    TM0,#32H      ;TIMER0 STOP
318                   ;
319                   LOAD_T0_L16 47,20
320 C120  E42FD5 @                LDM    T0LMD,#47
321 C123  E414D6 @                LDM    T0LLD,#20
322 C126  E400DA                  LDM    TM01,#00H
323 C129  E475D0                  LDM    TM0,#75H      ;COUNT, PS5(8uS)
```

GMS8xxxx Cross Assembler V1.55, By HYNIX Semiconductor, Inc.1995/12/12 14:59:46 (PAGE 6)

```
324 C12C   73CFFD            BBC     IRQT0,$
325 C12F   4BCF60            NOT1    IRQT0
326 C132   E432D0            LDM     TM0,#32H    ;TIMER0 STOP
327 C135   6F                RET
328                ;
329                ;============================================================
330                ;          DELAY  ROUTINE
331                ;============================================================
332                ;
333 C136   3E14    DELAY:    LDY     #20
334 C138   7BFE              DBNE    Y,$
335 C13A   6F                RET
336                ;
337                ;============================================================
338                ;          KEY  SCAN  ROUTINE
339                ;============================================================
340 C13B   FF      KSCN:  NOP
341 C13C   6F                RET
342                ;
343                          END
```

-- 0 Error(s) --

--- Total Machine Code : 345 Bytes --

2-3. M50560-001 FORMAT

2-3-1. Overview

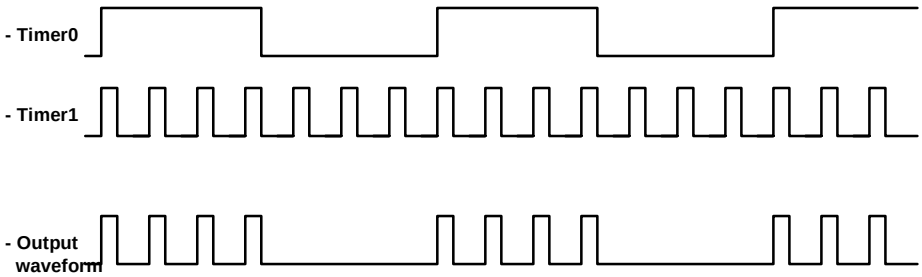
This format is made by using Timer0 & Timer1 for carrier. So, you can find out how carrier mode is made by Logic AND timer0 & Timer1

2-3-2. RAM Description

Label	Address	Description
KEY-NUMBER	$00H	Key data from key martix
OLDKEY-BUFFER	$02H	After signal at, storaging the data
DATA1	$Buffer + 1	Valueasle key data converted from Key number
M5CUSTOM	$Buffer	Valiable custom data converted from mode
SENDD	$04H	Data transfer
BUFFER	-	Data Buffer

2-3-3. Program Explanation

1) Duty : carrier mode is made for 1/3 duty by logic AND of Timer1 and Timer0

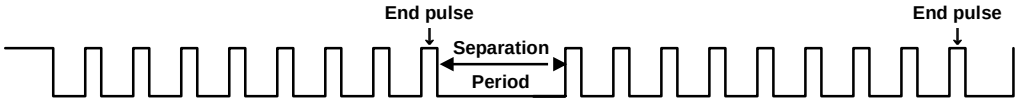


1) Head & Data

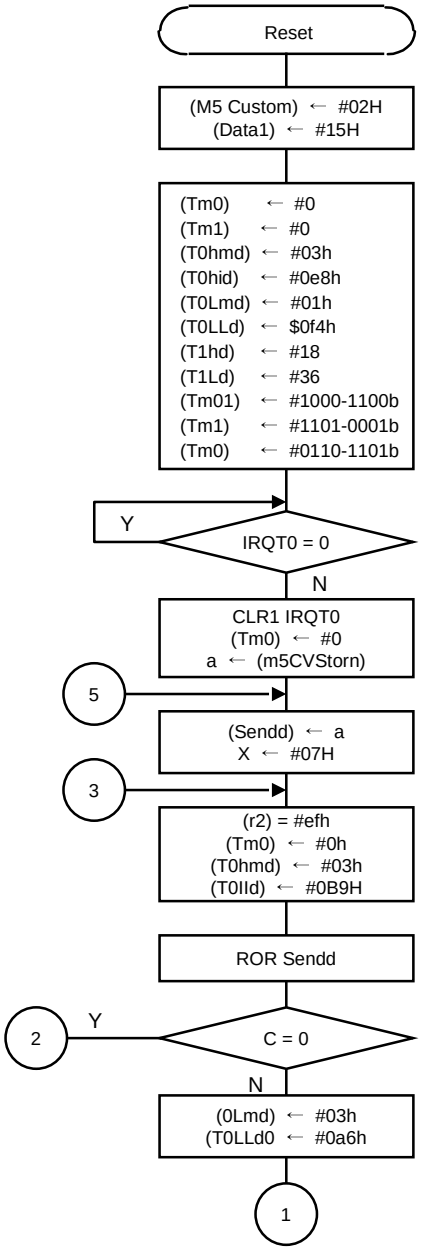
Head/Bit0/Bit1 is made by using Timer0 & Timer1. As for head, PS of Timer0 to changed to PS5, because it is too long to cover head high pulse(8ns). Ps of Timer1 is always fixed to PS1. When mainpulating bit, PS of Timer0 is change to PS1.

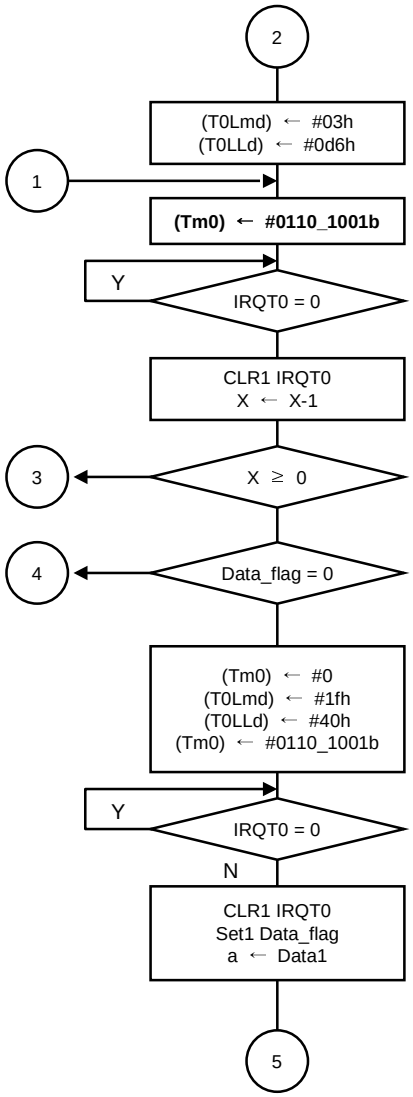
3) Seperation period & End pulse

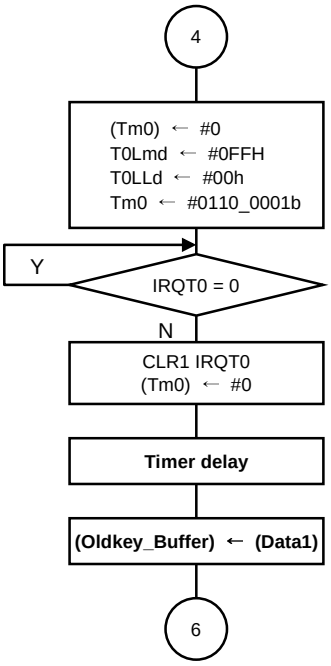
They are formed by changing Data register of Timer0 & Timer1



2-3-4. Flow Chart




2
(T0Lmd) ← #03h
(T0LLd) ← #0d6h
1
(Tm0) ← #0110_1001b
Y
IRQT0 = 0
CLR1 IRQT0
X ← X-1
3
X ≥ 0
: Manipulating 8bit is finished
4
Data_flag = 0
: Is all signal out completed?
(Tm0) ← #0
(T0Lmd) ← #1fh
(T0LLd) ← #40h
(Tm0) ← #0110_1001b
Y
IRQT0 = 0
N
CLR1 IRQT0
Set1 Data_flag
a ← Data1
5



:Data1 is stored for Keyscan

: Go to pre-stop routine

S8xxxx Cross Assembler V1.55, By HYNIX Semiconductor, Inc.1995/12/13 11:41:49 (PAGE 1)

```
1                 NOLIST
95              ;=============================================
96              ;
97              ;            M50560  TX  PROGRAM
98              ;
99              ;=============================================
100             ;=============================================
101             ;        RAM ALLOCATION
102             ;=============================================
103             ;
104             KEY_NUMBER  EQU    00H
105             FLAG        EQU    01H
106             DATA_FLAG   EQU    3,FLAG
107             OLDKEY_BUFFER EQU    02H
108             BUFFER      DS     4
109             DATA1       EQU    BUFFER+1
110             M5CUSTOM    EQU    BUFFER
111             DATA        EQU    03H
112             SENDD       EQU    04H
113             ;================================================
114             ;     MACRO SPACE
115             ;================================================
116             SAVE        MACRO
117                         PUSH   A
118                         PUSH   X
119                         PUSH   Y
120                         PUSH   PSW
121                         ENDM
122             RESET       MACRO
123                         POP    PSW
124                         POP    Y
125                         POP    X
126                         POP    A
127                         ENDM
128             ;
129             ;================================================
130             ;     INTERRUPT VECTOR ADDRESS TABLE
131             ;================================================
132                 ORG    0FFE6H
133 FFE6  00C0              DW     RESET      ;BITR
134 FFE8  00C0              DW     RESET      ;WDTR
135 FFEA  00C0              DW     RESET      ;NOT USED
136 FFEC  00C0              DW     RESET      ;NOT USED
137 FFEE  00C0              DW     RESET      ;TIMER2
138 FFF0  00C0              DW     RESET      ;TIMER1
139 FFF2  00C0              DW     RESET      ;TIMER0
```

GMS8xxxx Cross Assembler V1.55, By HYNIX Semiconductor, Inc.1995/12/13 11:41:49 (PAGE 2)

```
140 FFF4  00C0            DW       RESET              ;EXTERNAL INTERRUPT2
141 FFF6  00C0            DW       RESET              ;EXTERNAL INTERRUPT1
142 FFF8  00C0            DW       RESET              ;EXTERNAL INTERRUPT0
143 FFFA 00C0             DW       RESET              ;KEY SCAN
144 FFFC 00C0             DW       RESET              ;NOT USED
145 FFFE  00C0            DW       RESET              ;RESET
146                  ;================================================
147                  ;            MAIN PROGRAM
148                  ;================================================
149                  ;
150                  ORG            0C000H
151                  ;
152 C000  C400       RESET:  LDA  #0
153 C002  1E00             LDX      #0
154 C004  FB         CLEAR:  STA    {X}+              ; RAM  CLEAR
155 C005  5EC0             CMPX     #0C0H             ;
156 C007  70FB             BNE      CLEAR             ;
157 C009  1EFE             LDX      #0FEH             ;== STACK POINT INITIAL  0FEH
158 C00B  8E               TXSP                       ;
159                  ;== PORT INITIAL
160 C00C  E4FFDE AAA:    LDM    R1ODC,#0FFH     ;R1 ARE ALL OPEN DRAIN
161 C00F  E400C1         LDM      R0DD,#00H         ;R0 PORT IS INPUT
162 C012  E4FFC3         LDM      R1DD,#0FFH        ;R1 PORT IS OUTPUT
163 C015  E4FFC0         LDM      R0,#0FFH          ;R0 PORT IS ALL HIGH
164 C018  E4FFC2         LDM      R1,#0FFH          ;R1 PORT IS ALL HIGH
165 C01B  E41FC5         LDM      R2DD,#1FH         ;R2 PORT IS OUTPUT     ;
166 C01E  E41FC4         LDM      R2,#1FH           ;ALL LED OFF
167                   ;=== TIMER INITIAL
168 C021  E41DC7         LDM      CLKCTR,#0001_1101B   ;WDT OFF,IFBIT.,INTER T=(PS8)
169 C024  E4FFDC         LDM      SMRR0,#1111_1111B   ;R00~R07 STB MODE REL. BY KEY
170 C027  E480CE         LDM      IENH,#1000_0000B   ;KEYSCAN,TIMER2
171 C02A E400CC          LDM      IENL,#00H          ;WDTR,BITE = OFF
172 C02D E408D2          LDM      TM2,#0000_1000B  ;PS8(64US),COUNTING,T2 STOP
173 C030  E4FFC0         LDM      R0,#0FFH           ;R0 PORT IS INPUTED FROM R1
174 C033  E400C2         LDM      R1,#00H            ;R1 ALL LOW FOR DETECT KEY IN
175 C036  FF             NOP
176 C037  00             STOP
177 C038  FF             NOP
178 C039  F1CE           CLR1     IEKSCN
179 C03B E0              EI
180 C03C E40001          LDM      FLAG,#0
181 C03F E40000          LDM      KEY_NUMBER,#00H
182                  ;====== THIS ROUTINE IS ABOUT M50560
183 C042 E40200   M50560:  LDM    M5CUSTOM,#02H
184 C045 E40204          LDM      SENDD,#02H
185 C048 C900            LDY      KEY_NUMBER
```

GMS8xxxx Cross Assembler V1.55, By HYNIX Semiconductor, Inc.1995/12/13 11:41:49 (PAGE 3)

```
186 C04A  E41501          LDM    DATA1,#15H      ;(BUFFER+1 = DATA BUFFER)
187 C04D  7101            CLR1   DATA_FLAG
188 C04F  E400D0    HEAD: LDM    TM0,#0          ;TIMER0&1 IS STOPED.
189 C052  E400D1          LDM    TM1,#0          ;
190                 ;
191 C055  E403D3          LDM    T0HMD,#03H      ;8US*1000 = 8MS  ______
192 C058  E4E8D4          LDM    T0HLD,#0E8H     ;   " HEAD "      8MS  | 4MS
193 C05B  E401D5          LDM    T0LMD,#01H      ;8US*500  = 4MS       |____
194 C05E  E4F4D6          LDM    T0LLD,#0F4H     ;
195                 ;                                  ____
196 C061  E412D7          LDM    T1HD,#18        ; 9US        9US | 18US
197 C064  E424D8          LDM    T1LD,#36        ; 18US  " T =1:3" |______
198 C067  E48CDA          LDM    TM01,#1000_1100B   ;AND,T1&T2 O HIGH,TOUT
199                 ;
200 C06A  E4D1D1          LDM    TM1,#1101_0001B   ;0.5US,EV,MODUL,COUNT,T1 ST
201 C06D  E46DD0          LDM    TM0,#0110_1101B   ;8US,EV,MODUL,TIM ST,COUNT
202 C070  73CFFD          BBC    IRQT0,$           ;TILL INT.RQ.FLAG,NOSTOP LOOP
203 C073  71CF            CLR1   IRQT0
204 C075  E400D0          LDM    TM0,#0
205 C078  C500            LDA    M5CUSTOM
206 C07A  E504      SUB:  STA    SENDD
207 C07C  1E07            LDX    #07H
208 C07E  E400D0    ROUT: LDM    TM0,#0H         ;TIMER0 STOP
209 C081  E403D3          LDM    T0HMD,#03H      ;1. PULSE DEFINEING
210 C084  E4B9D4          LDM    T0HLD,#0B9H     ;0E8H
211                 ;                                  ;   "1000*0.5U=500US
212 C087  6904            ROR    SENDD           ;    C <- A.0
213 C089  5008            BCC    LOW
214 C08B  E40BD5    HIGH: LDM    T0LMD,#0BH      ;2. PULSE DEFINEING ___|    |
215 C08E  E4A6D6          LDM    T0LLD,#0A6H     ;   "3000*0.5US=1.5MS  |<-> |
216                 ;                                        |----|
217 C091  2F06            BRA    NEXT
218 C093  E403D5    LOW:  LDM    T0LMD,#03H      ;       //
219 C096  E4D6D6          LDM    T0LLD,#0D6H   ;    "1000*0.5US=500US
220 C099  E469D0    NEXT: LDM    TM0,#0110_1001B   ;PS1,EV,MODULE,COUNT,T0 STOP
221 C09C  73CFFD          BBC    IRQT0,$
222 C09F  71CF            CLR1   IRQT0
223 C0A1  FF              NOP
224 C0A2  AF              DEC    X
225 C0A3  10D9            BPL    ROUT
226 C0A5  630117          BBS    DATA_FLAG,DATAFINISH
227 C0A8  E400D0          LDM    TM0,#0
228 C0AB  E41FD5          LDM    T0LMD,#1FH      ;       //
229 C0AE  E440D6          LDM    T0LLD,#40H      ;    "1000*0.5US=500US
230 C0B1  E469D0          LDM    TM0,#0110_1001B   ;PS1,EV,SINGL,COUNT,T0 SART
231 C0B4  73CFFD          BBC    IRQT0,$
```

GMS8xxxx Cross Assembler V1.55, By HYNIX Semiconductor, Inc.1995/12/13 11:41:49 (PAGE 4)

```
232 C0B7   71CF          CLR1    IRQT0
233 C0B9   6101          SET1    DATA_FLAG
234 C0BB   C501          LDA     DATA1
235 C0BD   2FBB          BRA     SUB
236 C0BF   E400D0  DATAFINISH: LDM    TM0,#0
237 C0C2   E4FFD5        LDM     T0LMD,#0FFH
238 C0C5   E400D6        LDM     T0LLD,#00H          ; "1000*0.5US=500US
239 C0C8   E461D0        LDM     TM0,#0110_0001B     ;PS1,EV,SINGL,COUNT,T0 START
240 C0CB   73CFFD        BBC     IRQT0,$
241 C0CE   71CF          CLR1    IRQT0
242 C0D0   E400D0        LDM     TM0,#0
243 C0D3   E4A8D9        LDM     T2DR,#0A8H
244 C0D6   E41CD2        LDM     TM2,#0001_1100B     ;PS1,EV,SINGL,COUNT,T2 START
245 C0D9   33CFFD        BBC     IRQT2,$
246 C0DC   31CF          CLR1    IRQT2
247 C0DE   E400D2        LDM     TM2,#0
248 C0E1   C501          LDA     DATA1
249 C0E3   E502          STA     OLDKEY_BUFFER   ;DATA1=>OLDKEY_BUFFER
250 C0E5   1B0CC0        JMP     AAA
251                ;=============================================================
252                      END
```

-- 0 Error(s) --

--- Total Machine Code : 258 Bytes --

2-4. MV500 Flash Format

2-4-1. Overview

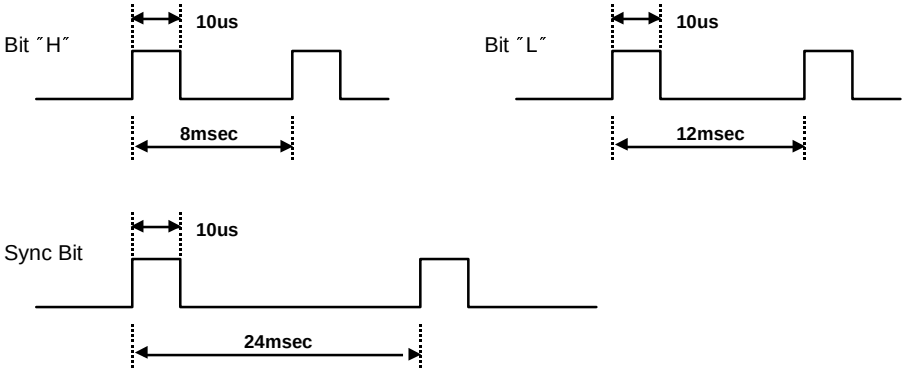
1) This module shows how to manipulat Timer0 and Timer1 interrupt request flag to achieve flash mode example
2) If does not use interrupt service routine

2-4-2. RAM Description

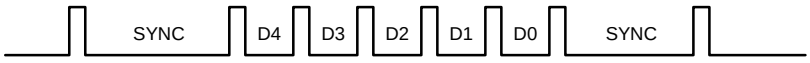
Label	Address	Description
KEY-DATA	$00h	valid key data come from key scan routine
TX-DATA	$01h	key data used in signal transmission routine
TX-FLAGS	$02h	flag used in transmission routine
RPT-FLAG	1, $02h	(active H), set to high to indicate repeat flame
EDGE-FLAG	0, $02h	dummy flag wait for same edge detect

2-4-3. Format description

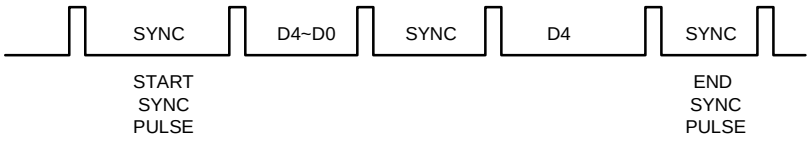
1) Bit definition



2) Configuration of flame

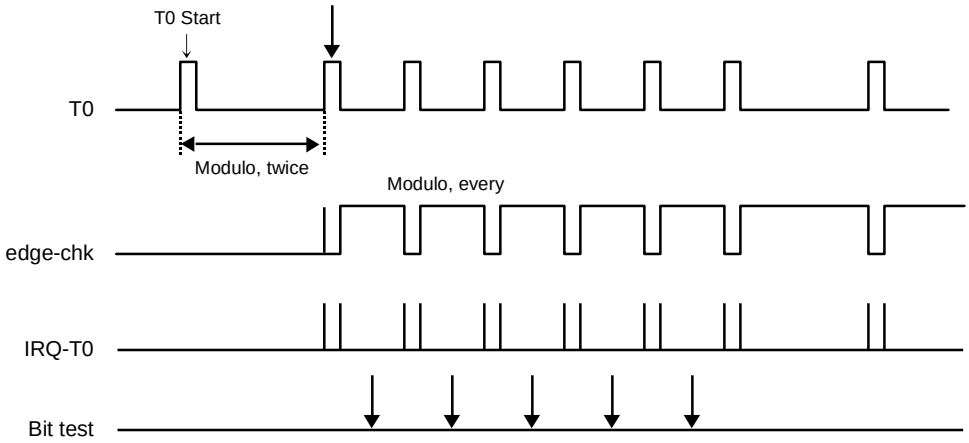


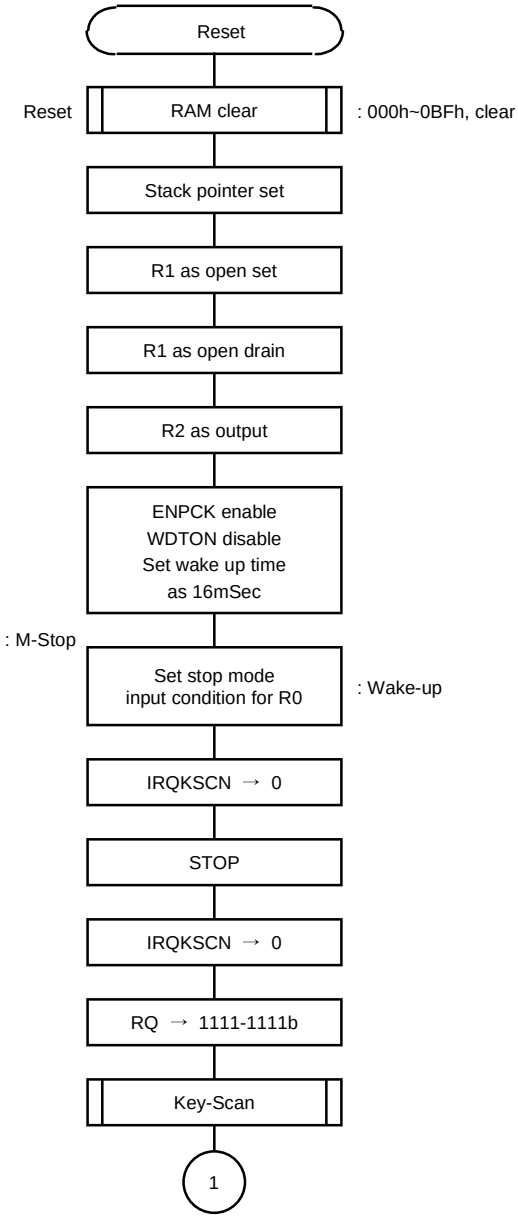
3) Flame interval : Waveform output is transmitted as long as key is depressed

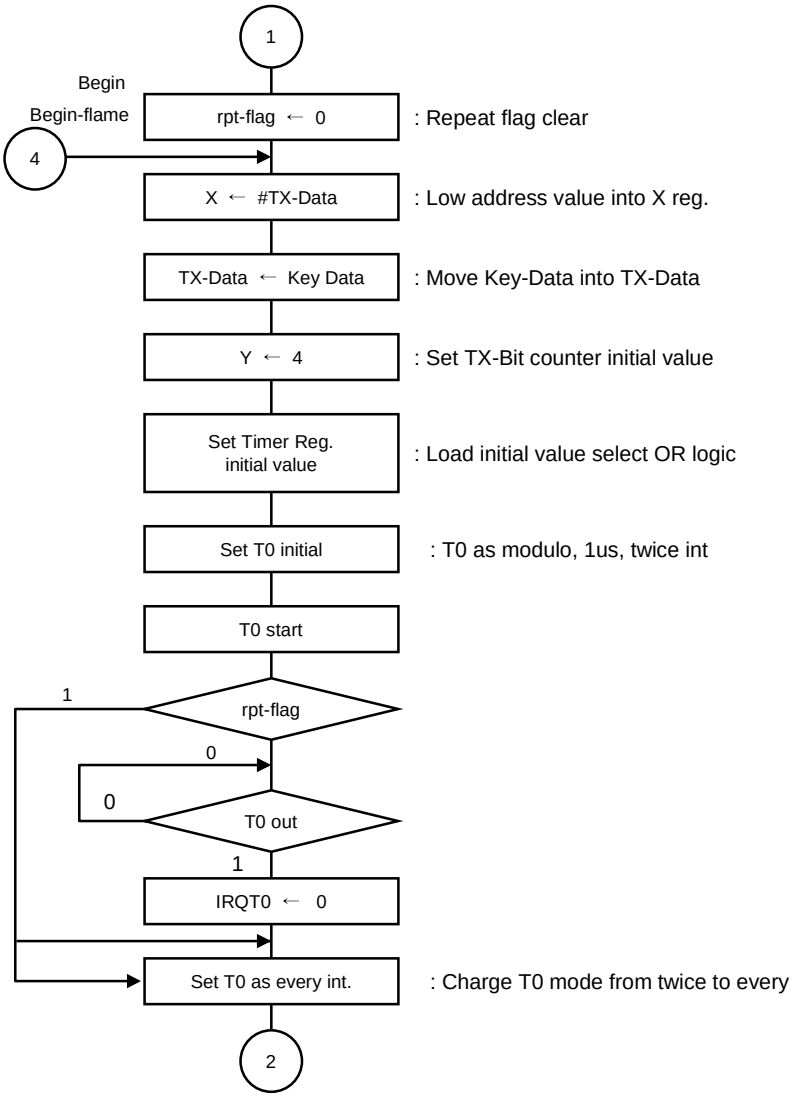


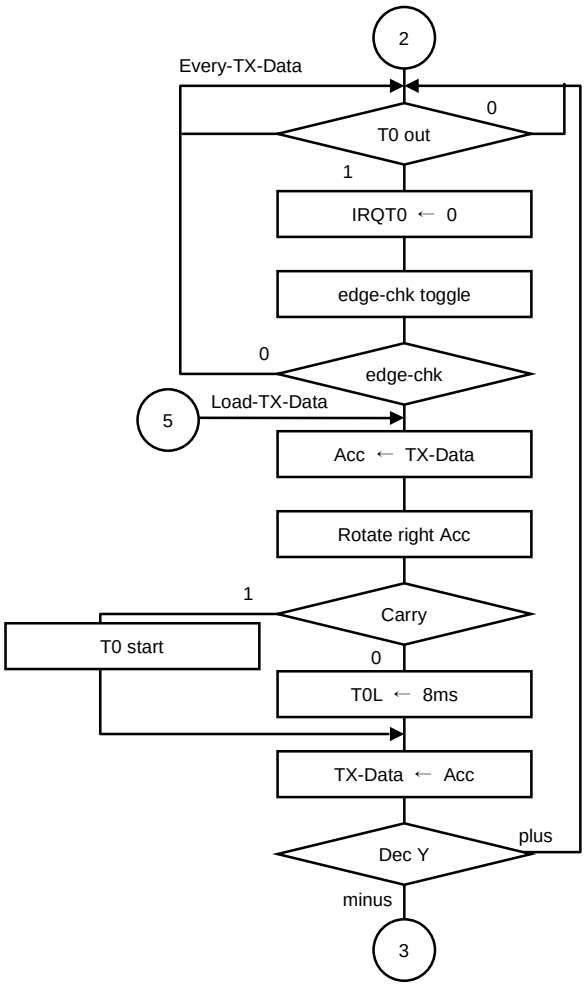
2-4-4. Module explanation

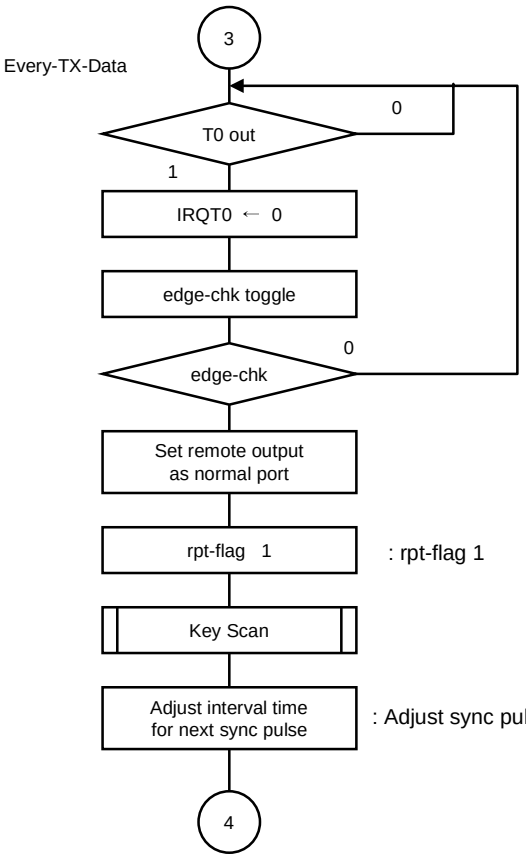
1) Timer0 is used to generate remote output signal
2) Timer1 is meaningless in this routine
3) Timer0 is selected as modulo, PS=1uS, twice interrupt during 1`st sync pulse generation
4) At the 1`st data bit, Timer0 mode is changed from twice interrupt to every interrupt
5) Edge-chk flag is used as toggle flag to distinguish same edge timming




Reset
Reset
RAM clear
: 000h~0BFh, clear
Stack pointer set
R1 as open set
R1 as open drain
R2 as output
ENPCK enable
WDTON disable
Set wake up time
as 16mSec
: M-Stop
Set stop mode
input condition for R0
: Wake-up
IRQKSCN → 0
STOP
IRQKSCN → 0
RQ → 1111-1111b
Key-Scan
1


1
Begin
Begin-flame
rpt-flag ← 0
: Repeat flag clear
4
X ← #TX-Data
: Low address value into X reg.
TX-Data ← Key Data
: Move Key-Data into TX-Data
Y ← 4
: Set TX-Bit counter initial value
Set Timer Reg.
initial value
: Load initial value select OR logic
Set T0 initial
: T0 as modulo, 1us, twice int
T0 start
1
rpt-flag
0
0
T0 out
1
IRQT0 ← 0
Set T0 as every int.
: Charge T0 mode from twice to every
2


2
Every-TX-Data
0
T0 out
1
IRQT0 ← 0
edge-chk toggle
0
edge-chk
: Wait for rising edge to rising edge
5
Load-TX-Data
Acc ← TX-Data
: Move TX-Data into Acc
Rotate right Acc
1
Carry
: Bit test
T0 start
0
T0L ← 8ms
: Bit0=12ms, Bit1=9ms
TX-Data ← Acc
plus
Dec Y
: Decrement TX-Bit counter
minus
3


3
Every-TX-Data
0
T0 out
1
IRQT0 ← 0
edge-chk toggle
0
edge-chk
Set remote output
as normal port
rpt-flag 1
: rpt-flag 1
Key Scan
Adjust interval time
for next sync pulse
: Adjust sync pulse interval as 24msec
4

GMS8xxxx Cross Assembler V1.55, By HYNIX Semiconductor, Inc.1995/12/12 15:03:59 (PAGE 1)

```
1               NOLIST
95          ;*************************************************************************
96          ;                                       *
97          ;           MV500 FLASH FORMAT                          *
98          ;                                       *
99          ;*************************************************************************
100         ;*************************************************************************
101         ;           RAM ALLOCATION AREA
102         ;*************************************************************************
103         KEY_DATA EQU    00H
104         TX_DATA  EQU    01H
105         TX_FLAGS EQU    02H
106         RPT_FLAG EQU    1,TX_FLAGS              ; REPEAT = 1
107         EDGE_CHK EQU    0,TX_FLAGS
108         ;
109         ;*************************************************************************
110         ;           SYMBOL DEFINED AREA
111         ;*************************************************************************
112         T0H_T1L_OR01 EQU    1000_1010B          ; INIT VALUE OF TIMER 0 = HIGH
113         ;               1 = LOW
114         ; TIMER 0/1 AS OR OUTPUT LOGIC
115         REM_AS_NORMAL EQU   0000_1010B      ; SET REMOTE OUTPUT AS NORMAL
116         T0_MOD_1US_TWICE EQU    0110_1010B  ; SET INT. ON TWICE OVF
117         T0_MOD_1US_EVERY EQU    0110_0010B  ; SET MODULO,1US, EVERY
118         ;*************************************************************************
119         ;           MACRO DEFINED AREA
120         ;*************************************************************************
121         LOAD_T0_H16 MACRO                       ; LOAD HIGH 16BIT DATA FOR T0
122                     LDM     T0HMD,#\1
123                     LDM     T0HLD,#\2
124                     ENDM
125         LOAD_T0_L16 MACRO                       ; LOAD LOW 16BIT DATA FOR T0
126                     LDM     T0LMD,#\1
127                     LDM     T0LLD,#\2
128                     ENDM
129         LOAD_T1_8 MACRO                         ; LOAD 8BIT DATA FOR T1
130                     LDM     T1HD,#\1
131                     LDM     T1LD,#\2
132                     ENDM
133         WAIT_INT_T0 MACRO
134                     BBC     IRQT0,$
135                     CLR1    RQT0
136                     ENDM
137         ;*************************************************************************
138         ;           INTERRUPT HANDLER AREA
139         ;*************************************************************************
```

GMS8xxxx Cross Assembler V1.55, By HYNIX Semiconductor, Inc.1995/12/12 15:03:59 (PAGE 2)

```
140                 ORG     0FFE4H
141           ;
142 FFE4    FF      UNUSE:  NOP
143 FFE5    7F              RETI
144           ;
145 FFE6    E4FF                DW      UNUSE                   ; BASIC INTERVAL TIMER
146 FFE8    00C0                DW      RESET                   ; WATCH DOG TIMER
147 FFEA    E4FF                DW      UNUSE                   ; A/D CON.
148 FFEC    E4FF                DW      UNUSE                   ; TIMER-3
149 FFEE    E4FF                DW      UNUSE                   ; TIMER-2
150 FFF0    E4FF                DW      UNUSE                   ; TIMER-1
151 FFF2    E4FF                DW      UNUSE                   ; TIMER-0
152 FFF4    E4FF                DW      UNUSE                   ; INT 3
153 FFF6    E4FF                DW      UNUSE                   ; INT 2
154 FFF8    E4FF                DW      UNUSE                   ; INT 1
155 FFFA    E4FF                DW      UNUSE                   ; KEY SCAN
156 FFFC    E4FF                DW      UNUSE
157 FFFE    00C0                DW      RESET                   ; RESET
158           ;*****************************************************************************
159           ;             MAIN   PROGRAM
160           ;*****************************************************************************
161                 ORG     0C000H
162           ;
163           ;---------------- RAM CLEAR, PORT INITIALIZING AND STOP -----------------
164           ;
165 C000    C400    RESET:  LDA     #0
166 C002    1E00            LDX     #0
167 C004    FB      RAMCLR: STA     {X}+
168 C005    5EC0            CMPX    #0C0H
169 C007    70FB            BNE     RAMCLR
170 C009    1EFE            LDX     #0FEH
171 C00B    8E              TXSP
172 C00C    E4FFDE          LDM     R1ODC,#1111_1111B   ; R1 AS OPEN DRAIN
173 C00F    E4FFC3          LDM     R1DD,#1111_1111B    ;
174 C012    E4FFC2          LDM     R1,#1111_1111B      ; R1 AS STROBE OUTPUT
175 C015    E41FC5          LDM     R2DD,#0001_1111B    ;
176 C018    E41FC4          LDM     R2,#0001_1111B      ; R2 AS OUTPUT
177           ;             LDM     CLKCTR,#0001_1101B    ; WDT_OFF, ENPCK_ON, 16MS
178 C01B    E480CE          LDM     IENH,#1000_0000B    ; KSCN
179           ;             LDM     IENL,#0100_0000B    ; WDT
180 C01E    E4FFDC  M_STOP: LDM     SMRR0,#1111_1111B   ; R00~7
181 C021    E400C2          LDM     R1,#00H             ; R10~7 STROBE ENABLE
182 C024    F1CF            CLR1    IRQKSCN
183 C026    00              STOP
184 C027    FF              NOP
185 C028    F1CF            CLR1    IRQKSCN
```

GMS8xxxx Cross Assembler V1.55, By HYNIX Semiconductor, Inc.1995/12/12 15:03:59 (PAGE 3)

```
186                     ;           EI
187 C02A   E4FFC2       LDM    R1,#1111_1111B          ; SET TO HIGH STROBE PORT
188 C02D   3B94C0       CALL   KEY_SCAN                ; DUMMY ROUTINE FOR
189                     ;                              ;      this example
190                     ;--------------- TRANSMITTING KEY DATA ---------------------------------
191                     ;
192 C030   E40002       BEGIN_TX: LDM    TX_FLAGS,#0   ; INITIALIZE TX_FLAGS
193 C033   1E01         BEGIN_FLAME: LDX    #TX_DATA    ; SET ADDRESS POINTER
194 C035   C500                  LDA    KEY_DATA       ; TX_DATA <--- KEY_DATA
195 C037   E501                  STA    TX_DATA        ;      IN KEY_SCAN
196 C039   3E04                  LDY    #4             ; TX BIT COUNTER = 5 TIMES
197                     LOAD_T0_H16 0,10               ; 10US PULSE WIDTH
198 C03B   E400D3 @              LDM    T0HMD,#0
199 C03E   E40AD4 @              LDM    T0HLD,#10
200                     LOAD_T0_L16 93,192             ; SYNC PULSE WIDTH = 24MS
201 C041   E45DD5 @              LDM      T0LMD,#93
202 C044   E4C0D6 @              LDM      T0LLD,#192
203 C047   E48ADA                LDM      TM01,#T0H_T1L_OR01
204 C04A   E46AD0                LDM      M0,#T0_MOD_1US_TWICE   ; MODULO, 1US, TWICE
205 C04D   230205                BBS      RPT_FLAG,SYNC_PLS
206                     WAIT_INT_T0
207 C050   73CFFD @              BBC      IRQT0,$
208 C053   71CF   @              CLR1     IRQT0
209 C055 E462D0   SYNC_PLS:      LDM      TM0,#T0_MOD_1US_EVERY   ; MODULO, 1US, EVERY
210                     ;
211                     LOOP_TX_DATA:    WAIT_INT_T0
212 C058   73CFFD @              BBC      IRQT0,$
213 C05B   71CF   @              CLR1     IRQT0
214 C05D   4B0200                NOT1     EDGE_CHK
215 C060   1302F5                BBC      EDGE_CHK,LOOP_TX_DATA
216 C063   BB           LOAD_TX_DATA: XMA    {X}
217 C064   68                    ROR      A               ;
218 C065   D008                  BCS      BIT_H           ; IF BIT IS HIGH
219                     BIT_L: LOAD_T0_L16 46,224        ; BIT 0 = 12MS
220 C067   E42ED5 @              LDM      T0LMD,#46
221 C06A   E4E0D6 @              LDM      T0LLD,#224
222 C06D   2F06                  BRA      SAVE_TX_DATA
223                     BIT_H: LOAD_T0_L16 31,64         ; BIT 1 = 8MS
224 C06F   E41FD5 @              LDM      T0LMD,#31
225 C072   E440D6 @              LDM      T0LLD,#64
226 C075   BB           SAVE_TX_DATA: XMA    {X}
227 C076   BE                    DEC      Y
228 C077   10DF                  BPL      LOOP_TX_DATA   ; 5BIT TX IS OVER
229                     END_TX_DATA: WAIT_INT_T0
230 C079 73CFFD @                BBC      IRQT0,$
231 C07C 71CF   @                CLR1     IRQT0
```

GMS8xxxx Cross Assembler V1.55, By HYNIX Semiconductor, Inc.1995/12/12 15:03:59 (PAGE 4)

```
232 C07E   4B0200              NOT1    EDGE_CHK
233 C081   1302F5              BBC     EDGE_CHK,END_TX_DATA
234 C084   E40ADA              LDM     TM01,#REM_AS_NORMAL   ; REMOUT AS NORMAL PORT
235 C087   2102                SET1    RPT_FLAG        ; SET REPEAT FLAG
236 C089   3B94C0              ALL     KEY_SCAN        ; DUMMY ROUTINE
237                    LOAD_T0_L16 93,192              ; SYNC PULSE WDITH= 24MS
238 C08C   E45DD5 @            LDM     T0LMD,#93
239 C08F   E4C0D6 @            LDM     T0LLD,#192
240 C092   2F9F                BRA     BEGIN_FLAME    REPEAT FLAME
241                    ;
242 C094   6F          KEY_SCAN: RET
243                            END
244                    ;
```

-- 0 Error(s) --

--- Total Machine Code : 177 Bytes --

2-5. SL490

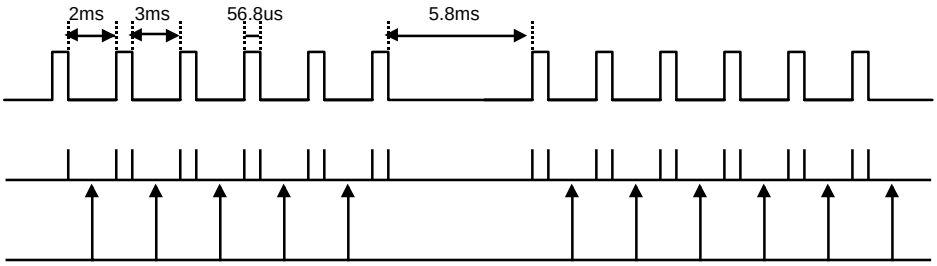
2-5-1. Overview

1) This program is example for SL490 waveform
2) It shows the method of making flash format that used by Timer0

2-5-2. Register Description

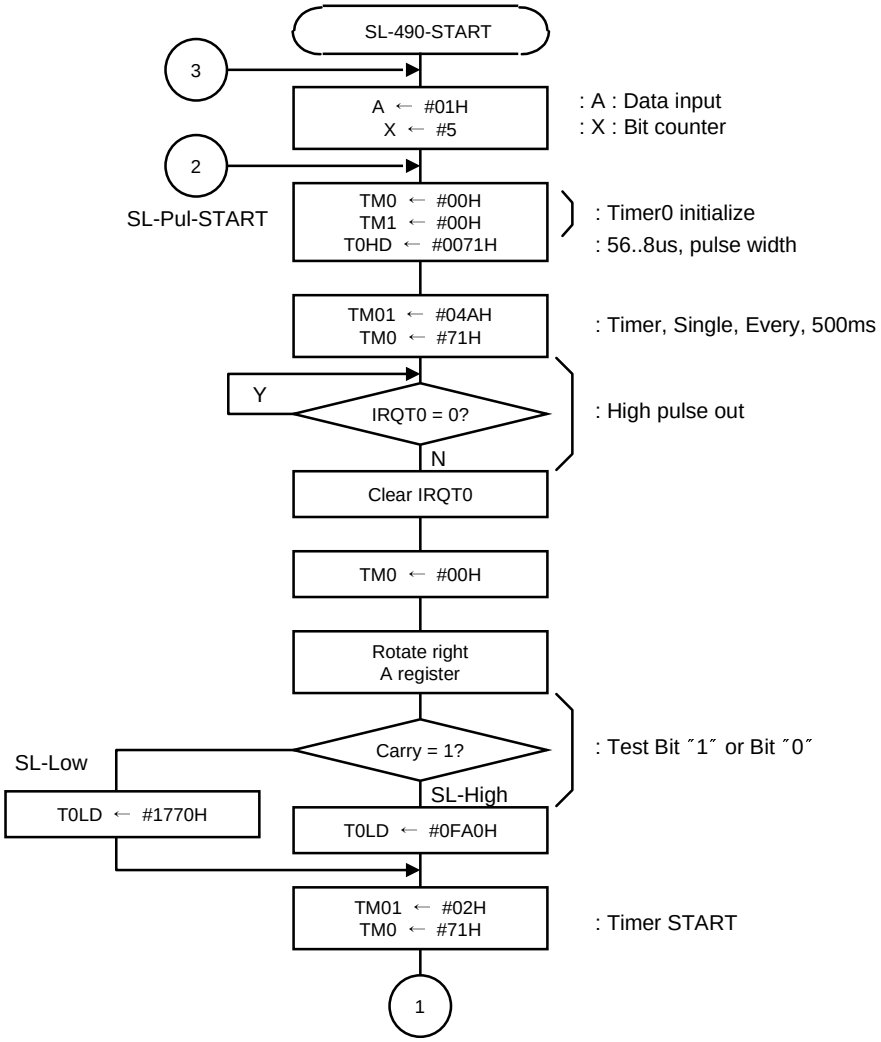
A register	Data Save (#01H)
X regoster	Bit Counter

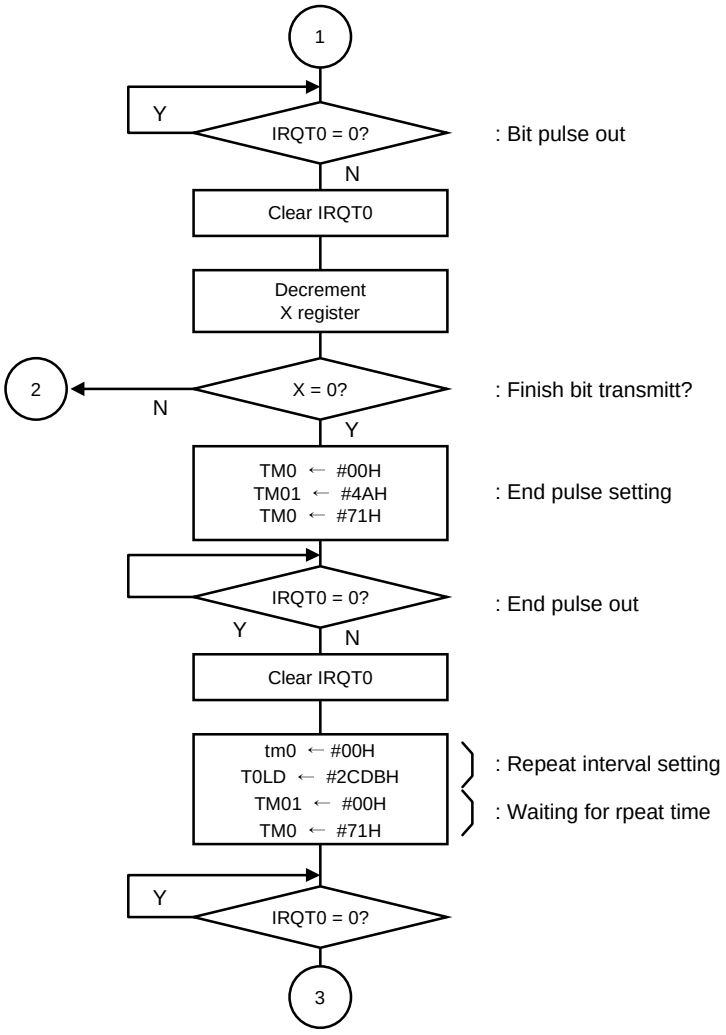
2-5-3. Pulse Description



2-5-4. Module explanation

1) Timer0 is used to generate remote output signal
2) Timer1 is meaningless in this routine
3) Timer0 mode register is used only single mode
4) It can be modified other method. Some relation example is MV500 flash format


SL-490-START
3
A ← #01H
X ← #5
: A : Data input
: X : Bit counter
2
SL-Pul-START
TM0 ← #00H
TM1 ← #00H
T0HD ← #0071H
: Timer0 initialize
: 56..8us, pulse width
TM01 ← #04AH
TM0 ← #71H
: Timer, Single, Every, 500ms
Y
IRQT0 = 0?
: High pulse out
N
Clear IRQT0
TM0 ← #00H
Rotate right
A register
Carry = 1?
: Test Bit ″1″ or Bit ″0″
SL-Low
SL-High
T0LD ← #1770H
T0LD ← #0FA0H
TM01 ← #02H
TM0 ← #71H
: Timer START
1


1
Y
IRQT0 = 0?
: Bit pulse out
N
Clear IRQT0
Decrement
X register
2
X = 0?
: Finish bit transmitt?
N
Y
TM0 ← #00H
TM01 ← #4AH
TM0 ← #71H
: End pulse setting
IRQT0 = 0?
: End pulse out
Y
N
Clear IRQT0
tm0 ← #00H
T0LD ← #2CDBH
TM01 ← #00H
TM0 ← #71H
: Repeat interval setting
: Waiting for rpeat time
Y
IRQT0 = 0?
3

GMS8xxxx Cross Assembler V1.55, By HYNIX Semiconductor, Inc.1995/12/07 18:27:55 (PAGE 1)

```
1                NOLIST
95               ;*****************************************************************************
96               ;
97               ;          WAVE FORMAT FOR SL490
98               ;
99               ;*****************************************************************************
100              ;*****************************************************************************
101              ;          RAM ALLOCATION AREA
102              ;*****************************************************************************
103              ;*****************************************************************************;
104              ;          INT VECTOR DEFINITION
105              ;*****************************************************************************
106              ;
107              ORG    0FFE6H
108              ;
109 FFE6  94C0          DW     UNUSE            ; BASIC INTERVAL TIMER
110 FFE8  94C0          DW     UNUSE            ; WATCH DOG TIMER
111 FFEA  94C0          DW     UNUSE            ; A/D CON.
112 FFEC  94C0          DW     UNUSE            ; TIMER-3
113 FFEE  94C0          DW     UNUSE            ; TIMER-2
114 FFF0  94C0          DW     UNUSE            ; TIMER-1
115 FFF2  94C0          DW     UNUSE            ; TIMER-0
116 FFF4  94C0          DW     UNUSE            ; INT 3
117 FFF6  94C0          DW     UNUSE            ; INT 2
118 FFF8  94C0          DW     UNUSE            ; INT 1
119 FFFA  94C0          DW     UNUSE            ; KEY SCAN
120 FFFC  94C0          DW     UNUSE
121 FFFE  00C0          DW     RESET
122
123              ;*****************************************************************************
124              ;          MACRO DEFINITION
125              ;*****************************************************************************
126              SAVE    MACRO
127                      PUSH   A
128                      PUSH   X
129                      PUSH   Y
130                      PUSH   PSW
131                      ENDM
132
133              RESTORE  MACRO
134                      POP    PSW
135                      POP    Y
136                      POP    X
137                      POP    A
138                      ENDM
139          ;*****************************************************************************
```

GMS8xxxx Cross Assembler V1.55, By HYNIX Semiconductor, Inc.1995/12/07 18:27:55 (PAGE 2)

```
140                 ;           MAIN PROGRAM
141                 ;*************************************************************************
142                             ORG    0C000H
143 C000    C400    RESET:   LDA    #0
144 C002    1E00             LDX    #0                      ; RAM CLEAR
145 C004    FB      RAMCLR:  STA    {X}+
146 C005    5EC0             CMPX   #0C0H
147 C007    70FB             BNE    RAMCLR
148 C009    1EFE             LDX    #0FEH
149 C00B    8E               TXSP                           ; STACK POINTER INITIALIZE
150 C00C    60               DI
151 C00D    E4FFDE           LDM    R1ODC,#1111_1111B       ; R1 AS OPEN DRAIN
152 C010    E4FFC3           LDM    R1DD,#1111_1111B        ; OUTPUT PORT
153 C013    E4FFC2           LDM    R1,#1111_1111B
154 C016    E480CE           LDM    IENH,#1000_0000B        ; KSCN ENABLE
155 C019    E41FC5           LDM    R2DD,#0001_1111B        ;
156 C01C    E41FC4           LDM    R2,#0001_1111B          ; R2 AS OUTPUT
157 C01F    E4FFDC           LDM    SMRR0,#1111_1111B       ; KEY SCAN RELEASE
158                 ; BY R00~07
159 C022    E41DC7           LDM    CLKCTR,#0001_1101B ; WDT_OFF, ENPCK_OFF, 16MS(PS8)
160 C025    E400C2           LDM    R1,#00H                 ; R10 ~ R15 STROBE ENABLE
161 C028    F1CF             CLR1   IRQKSCN
162 C02A    00               STOP
163 C02B    FF               NOP
164 C02C    E4FFC2           LDM    R1,#1111_1111B
165                 ;           CALL    KEY_SCAN
166
167
168                 ;*************************************************************************
169                 ;           TRANSMITTING KEY DATA
170                 ;*************************************************************************
171                 ;*************************************************************************
172                 ;           FLASH PULSE: SL490
173                 ;*************************************************************************
174 C02F    C401    SL490_START: LDA    #01H               ;KEY DATA INPUT
175 C031    1E05             LDX    #5
176
177 C033    E400D0  SL_PUL_START: LDM    TM0,#00H          ;TIMER STOP &INITIALIZE
178 C036    E400D1           LDM    TM1,#00H
179 C039    E400D3           LDM    T0HMD,#00H             ;56.8US,PULSE_HIGH WIDTH
180 C03C    E471D4           LDM    T0HLD,#71H             ;500NS*113=56.8US
181 C03F    E44ADA           LDM    TM01,#0100_1010B       ;TIM,STA,CON,SING,EVE,500NS
182 C042    E471D0           LDM    TM0,#0111_0001B        ;PULSE OUT START
183 C045    73CFFD           BBC    IRQT0,$                ;TOUT,HIGH,EQ,T0HIGH,
184 C048    71CF             CLR1   IRQT0
185 C04A    E400D0           LDM    TM0,#00H               ;TIMER STOP &INITIALIZE
```

GMS8xxxx Cross Assembler V1.55, By HYNIX Semiconductor, Inc.1995/12/07 18:27:55 (PAGE 3)

```
186 C04D   68                ROR     A
187 C04E   5008              BCC     SL_LOW
188 C050   E40FD5            LDM     T0LMD,#0FH        ;0.5US*4000=2MS
189 C053   E4A0D6            LDM     T0LLD,#0A0H
190 C056   2F08              BRA     SLPULSE_OUT
191
192 C058   E417D5  SL_LOW:   LDM     T0LMD,#17H        ;0.5US*6000=3MS
193 C05B   E470D6            LDM     T0LLD,#70H
194 C05E   2F00              BRA     SLPULSE_OUT
195
196 C060   E402DA  SLPULSE_OUT: LDM   TM01,#0000_0010B  ;TIM,STA,CON,SING,EVE,500NS
197 C063   E471D0            LDM     TM0,#0111_0001B   ;PULSE OUT START
198
199 C066   73CFFD            BBC     IRQT0,$           ;TOUT,HIGH,EQ,T0HIGH,
200 C069   71CF              CLR1    IRQT0
201 C06B   AF                DEC     X
202 C06C   5E00              CMPX    #0
203 C06E   70C3              BNE     SL_PUL_START
204 C070   E400D0            LDM     TM0,#00H          ;END PULSE OUT
205 C073   E44ADA            LDM     TM01,#0100_1010B
206 C076   E471D0            LDM     TM0,#0111_0001B   ;TIM,STA,CONT,SING,EVE,500NS
207
208 C079   73CFFD            BBC     IRQT0,$
209 C07C   71CF              CLR1    IRQT0
210 C07E   E400D0            LDM     TM0,#00H
211 C081   E42CD5            LDM     T0LMD,#2CH
212 C084   E4D8D6            LDM     T0LLD,#0D8H
213 C087   E400DA            LDM     TM01,#00H
214 C08A   E471D0            LDM     TM0,#0111_0001B   ;REPEAT DATA SETTING
215 C08D   73CFFD            BBC     IRQT0,$
216 C090   71CF              CLR1    IRQT0
217 C092   2F9B              BRA     SL490_START
218
219
220
221 C094   FF        UNUSE:  NOP
222 C095   7F                RETI
223                          END
```

-- 0 Error(s) --

--- Total Machine Code : 176 Bytes --

2-6. IRT1260

2-6-1. Overview

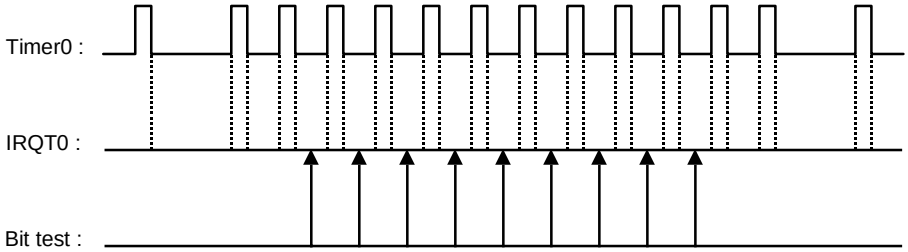
1) This program is example for irt1260
2) It shows the method of making flash format that used by Timer0

2-6-2. RAM Description

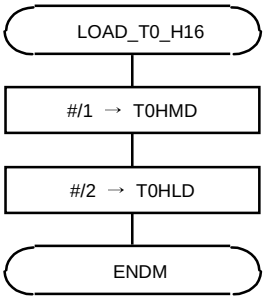
Label	Address	Description
NEWKEY	$03h	Valid key data come from key scan routine
IRT FLAG	4, $08h	Repeat flag
BUFFER	$0Bh	Key data
BUFFER1	]$0Ch	System data

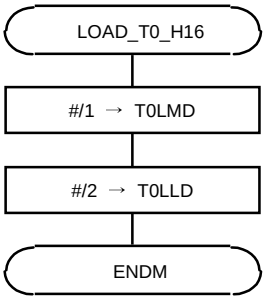
2-6-3. Pulse Description

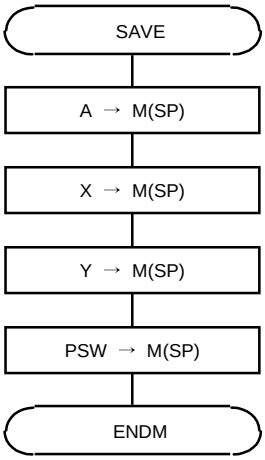
1) Timer0 is used to generate remote output signal
2) Timer0 is modulo-N mode, interrupt every counter overflow
3) Timer1 is meaningless in this routine

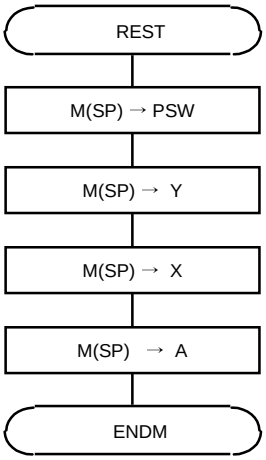


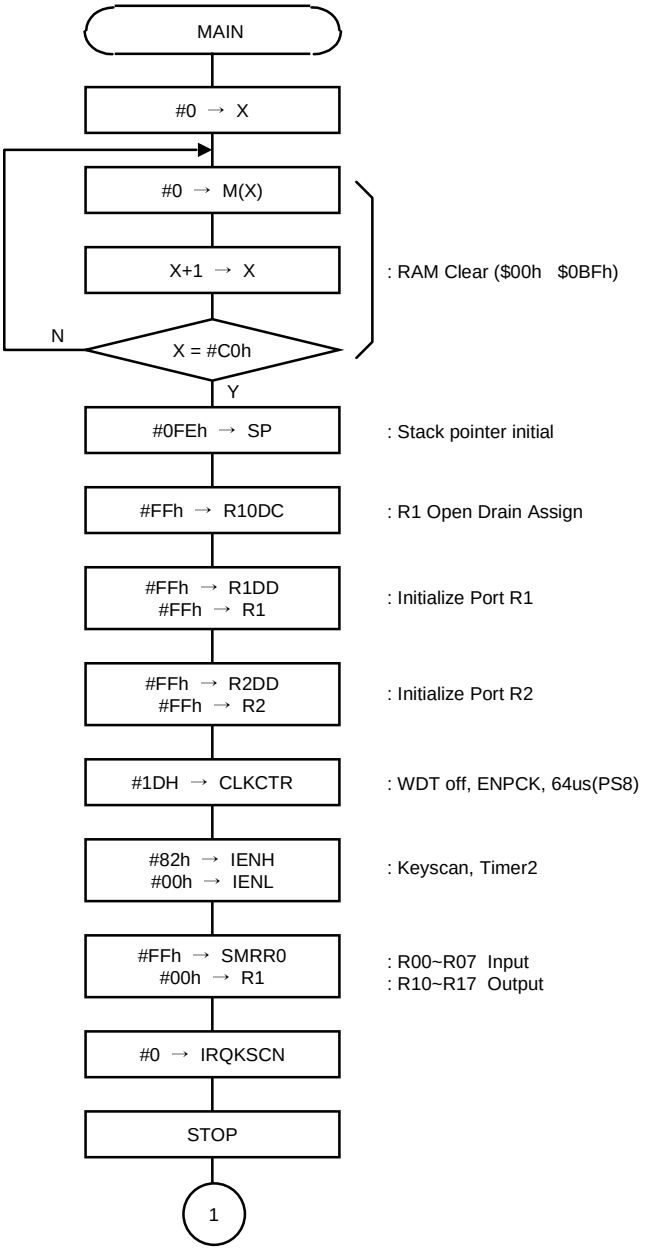
2-6-4. Flow Chart

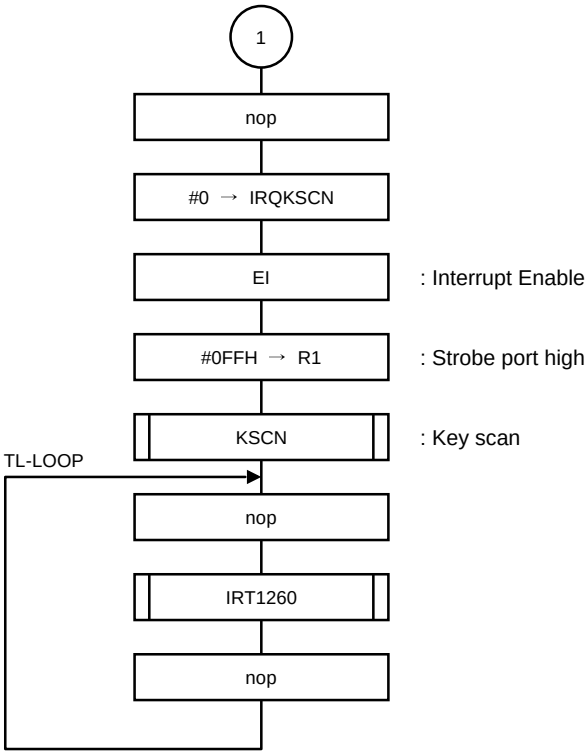


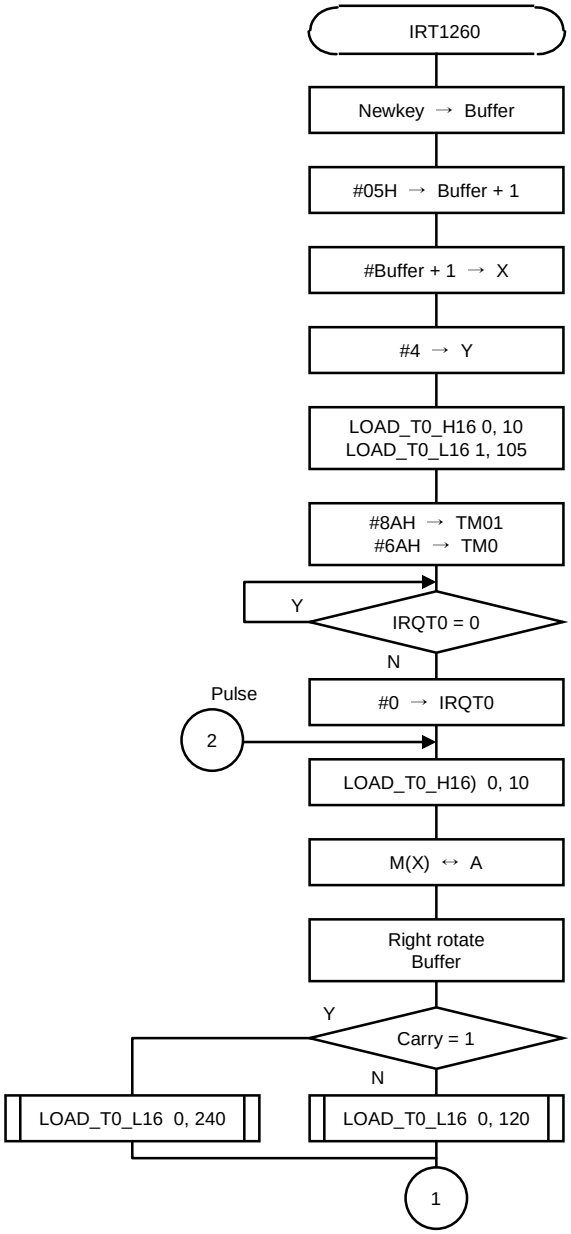


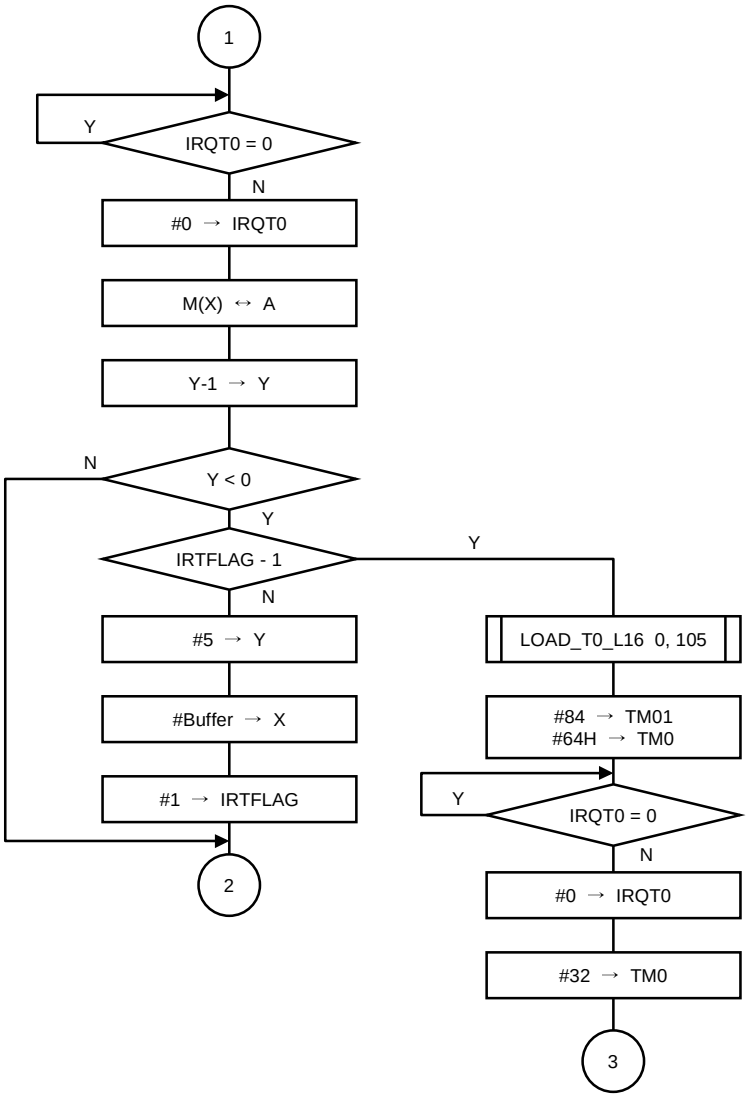


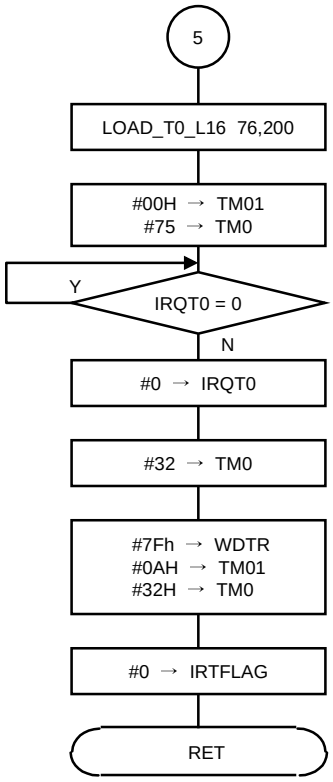



MAIN
#0 → X
#0 → M(X)
X+1 → X
: RAM Clear ($00h $0BFh)
N
X = #C0h
Y
#0FEh → SP
: Stack pointer initial
#FFh → R10DC
: R1 Open Drain Assign
#FFh → R1DD
#FFh → R1
: Initialize Port R1
#FFh → R2DD
#FFh → R2
: Initialize Port R2
#1DH → CLKCTR
: WDT off, ENPCK, 64us(PS8)
#82h → IENH
#00h → IENL
: Keyscan, Timer2
#FFh → SMRR0
#00h → R1
: R00~R07 Input
: R10~R17 Output
#0 → IRQKSCN
STOP
1


1
nop
#0 → IRQKSCN
EI
: Interrupt Enable
#0FFH → R1
: Strobe port high
KSCN
: Key scan
TL-LOOP
nop
IRT1260
nop


IRT1260
Newkey → Buffer
#05H → Buffer + 1
#Buffer + 1 → X
#4 → Y
LOAD_T0_H16 0, 10
LOAD_T0_L16 1, 105
#8AH → TM01
#6AH → TM0
Y
IRQT0 = 0
N
Pulse
2
#0 → IRQT0
LOAD_T0_H16) 0, 10
M(X) ↔ A
Right rotate
Buffer
Y
Carry = 1
N
LOAD_T0_L16 0, 240
LOAD_T0_L16 0, 120
1


1
Y
IRQT0 = 0
N
#0 → IRQT0
M(X) ↔ A
Y-1 → Y
N
Y < 0
Y
IRTFLAG - 1
Y
N
#5 → Y
#Buffer → X
#1 → IRTFLAG
2
LOAD_T0_L16 0, 105
#84 → TM01
#64H → TM0
Y
IRQT0 = 0
N
#0 → IRQT0
#32 → TM0
3


5
LOAD_T0_L16 76,200
#00H → TM01
#75 → TM0
Y
IRQT0 = 0
N
#0 → IRQT0
#32 → TM0
#7Fh → WDTR
#0AH → TM01
#32H → TM0
#0 → IRTFLAG
RET

GMS8xxxx Cross Assembler V1.55, By HYNIX Semiconductor, Inc.1995/12/12 17:37:30 (PAGE 1)

```
1               NOLIST
95          ;=====================================================================
96          ;
97          ;           IRT1260  TX PROGRAM
98          ;
99          ;=====================================================================
100         ;=====================================================================
101         ;           RAM  ALLOCATION
102         ;=====================================================================
103         ;
104         NEWKEY      EQU    03H              ;NEW KEY NUMBER
105         IRTFLAG     EQU    4,08H            ;IRT1260 FLAG
106         BUFFER      EQU    0BH              ;KEY DATA TX RAM
107         BUFFER1     EQU    0CH              ;SYSTEM DATA TX RAM
108         ;
109         ;=====================================================================
110         ;           MACRO  DEFINITION
111         ;=====================================================================
112         LOAD_T0_H16 MACRO                   ;LOAD HIGH_DATA FOR TIMER0
113                     LDM    T0HMD,#\1
114                     LDM    T0HLD,#\2
115                     ENDM
116         ;
117         LOAD_T0_L16 MACRO                   ;LOAD LOW_DATA FOR TIMER0
118                     LDM    T0LMD,#\1
119                     LDM    T0LLD,#\2
120                     ENDM
121         ;
122         SAVE    MACRO                       ;REGISTER SAVE
123                     PUSH   A
124                     PUSH   X
125                     PUSH   Y
126                     PUSH   PSW
127                     ENDM
128         ;
129         REST    MACRO                       ;REGISTER RESTORE
130                     POP    PSW
131                     POP    Y
132                     POP    X
133                     POP    A
134                     ENDM
135         ;
136         ;=====================================================================
137         ;           INTERRUPT  VECTOR  TABLE
138         ;=====================================================================
139         ;
```

GMS8xxxx Cross Assembler V1.55, By HYNIX Semiconductor, Inc.1995/12/12 17:37:30 (PAGE 2)

```
140                             ORG    0FFE4H
141                     ;
142 FFE4   FF       NOTUSE:     NOP
143 FFE5   7F                   RETI
144                     ;
145 FFE6   E4FF                 DW     NOTUSE          ; BASIC INTERVAL TIMER
146 FFE8   E4FF                 DW     NOTUSE          ; WATCH DOG TIMER
147 FFEA   E4FF                 DW     NOTUSE          ; A/D CONVERTER
148 FFEC   E4FF                 DW     NOTUSE          ; TIMER-3
149 FFEE   E4FF                 DW     NOTUSE          ; TIMER-2
150 FFF0   E4FF                 DW     NOTUSE          ; TIMER-1
151 FFF2   E4FF                 DW     NOTUSE          ; TIMER-0
152 FFF4   E4FF                 DW     NOTUSE          ; INT 3
153 FFF6   E4FF                 DW     NOTUSE          ; INT 2
154 FFF8   E4FF                 DW     NOTUSE          ; INT 1
155 FFFA   E4FF                 DW     NOTUSE          ; KEY SCAN
156 FFFC   E4FF                 DW     NOTUSE
157 FFFE   00C0                 DW     MAIN            ; RESET
158                     ;
159                     ;================================================================
160                     ;           MAIN  PROGRAM
161                     ;================================================================
162                     ;
163                             ORG    0C000H
164 C000   1E00                 MAIN:   LDX    #0
165 C002   C400                 LDA    #0               ;RAM CLEAR(!0000H->!00BFH)
166 C004   FB       CLR:        STA    {X}+
167 C005   5EC0                 CMPX   #0C0H
168 C007   70FB                 BNE    CLR
169 C009   1EFE                 LDX    #0FEH            ;STACK POINTER INITIAL
170 C00B   8E                   TXSP
171 C00C   E4FFDE               LDM    R1ODC,#0FFH      ;R1 OPEN DRAIN ASSIGN REG.
172 C00F   E4FFC3               LDM    R1DD,#0FFH       ;DATA DIRECTION REG.
173 C012   E4FFC2               LDM    R1,#0FFH         ;R1 DATA REG.
174 C015   E41FC5               LDM    R2DD,#1FH        ;DATA DIRECTION REG.
175 C018   E41FC4               LDM    R2,#1FH          ;R2 DATA REG. OUTPUT
176 C01B   E41DC7               LDM    CLKCTR,#1DH      ;WDT OFF, ENPCK, 64uS(PS8)
177 C01E   E480CE               LDM    IENH,#80H        ;KEYSCAN
178 C021   E400CC               LDM    IENL,#00H        ;WATCH DOG TIMER
179 C024   E4FFDC               LDM    SMRR0,#0FFH      ;R00~7 INPUT
180 C027   E400C2               LDM    R1,#00H          ;R10~7 STROBE ENABLE(OUTPUT)
181 C02A   F1CF                 CLR1   IRQKSCN
182 C02C   00                   STOP
183          ;
184 C02D   FF                   NOP
185 C02E   F1CF                 CLR1   IRQKSCN
```

GMS8xxxx Cross Assembler V1.55, By HYNIX Semiconductor, Inc.1995/12/12 17:37:30 (PAGE 3)

```
186 C030   E0                  EI
187 C031   E4FFC2              LDM    R1,#0FFH          ;STROBE PORT HIGH
188 C034   3BC9C0              CALL   KSCN              ;TEST IF KEY PRESSED
189 C037   FF      TX_LOOP:    NOP
190 C038   3B3EC0              CALL   IRT1260
191 C03B   FF                  NOP
192 C03C   2FF9                BRA    TX_LOOP
193                    ;
194                    ;=========================================================
195                    ;           IRT1260  TX  ROUTINE
196                    ;=========================================================
197                    ;
198 C03E   C503        IRT1260: LDA    NEWKEY           ;IRT1260 FLASH
199 C040   E50B                 STA    BUFFER           ;
200 C042   E4050C               LDM    BUFFER+1,#05H    ;FIXED SYSTEM
201 C045   1E0C                 LDX    #BUFFER+1        ;
202 C047   3E04                 LDY    #4
203                             LOAD_T0_H16 0,10         ;10uS PULSE
204 C049   E400D3 @             LDM    T0HMD,#0
205 C04C   E40AD4 @             LDM    T0HLD,#10
206                    LOAD_T0_L16 1,105                ;START SYNC PULSE = 360uS
207 C04F   E401D5 @             LDM    T0LMD,#1
208 C052   E469D6 @             LDM    T0LLD,#105
209 C055   E48ADA               LDM    TM01,#8AH
210 C058   E46AD0               LDM    TM0,#6AH         ;1uS
211 C05B   73CFFD               BBC    IRQT0,$
212 C05E   4BCF60               NOT1   IRQT0
213                    ;
214                    PULSE: LOAD_T0_H16 0,10          ;10uS PULSE
215 C061   E400D3 @             LDM    T0HMD,#0
216 C064   E40AD4 @             LDM    T0HLD,#10
217 C067   BB                   XMA    {X}
218 C068   68                   ROR    A                ;
219 C069   D008                 BCS    HIGH
220          LOAD_T0_L16 0,120          ;BIT 0 = 120uS
221 C06B   E400D5 @             LDM    T0LMD,#0
222 C06E   E478D6 @             LDM    T0LLD,#120
223 C071   2F06                 BRA    LOW
224                    ;
225                    HIGH: LOAD_T0_L16 0,240          ;BIT 1 = 240uS
226 C073   E400D5 @             LDM    T0LMD,#0
227 C076   E4F0D6 @             LDM    T0LLD,#240
228 C079   73CFFD      LOW:     BBC    IRQT0,$
229 C07C   4BCF60               NOT1   IRQT0
230 C07F   BB                   XMA    {X}
231 C080   BE                   DEC    Y
```

GMS8xxxx Cross Assembler V1.55, By HYNIX Semiconductor, Inc.1995/12/12 17:37:30 (PAGE 4)

```
232 C081   10DE              BPL    PULSE          ;5BIT TX COMPLETE
233                     ;
234 C083   830808            BBS    IRTFLAG,LOOP
235 C086   3E05              LDY    #5
236 C088   1E0B              LDX    #BUFFER
237 C08A   8108              SET1   IRTFLAG        ;
238 C08C   2FD3              BRA    PULSE
239                     LOOP: LOAD_T0_L16 1,105     ;SYNC PULSE = 360uS
240 C08E   E401D5 @          LDM    T0LMD,#1
241 C091   E469D6 @          LDM    T0LLD,#105
242 C094   E48ADA            LDM    TM01,#8AH
243 C097   E46AD0            LDM    TM0,#6AH       ;1uS
244 C09A   73CFFD            BBC    IRQT0,$
245 C09D   4BCF60            NOT1   IRQT0          ;FIRST DATA BIT PULSE
246 C0A0   E432D0            LDM    TM0,#32H       ;TIMER0 STOP
247                     LOAD_T0_L16 76,200          ;TIME WAIT
248 C0A3   E44CD5 @          LDM    T0LMD,#76
249 C0A6   E4C8D6 @          LDM    T0LLD,#200
250 C0A9   E400DA            LDM    TM01,#00H
251 C0AC   E475D0            LDM    TM0,#75H       ;COUNT, PS5(8uS)
252 C0AF   73CFFD            BBC    IRQT0,$
253 C0B2   4BCF60            NOT1   IRQT0
254 C0B5   E432D0            LDM    TM0,#32H       ;TIMER0 STOP
255 C0B8   E47FC8            LDM    WDTR,#7FH      ;WDTR CLEAR
256 C0BB   E40ADA            LDM    TM01,#0AH      ;REMOTE OUTPUT AS NORMAL PORT
257 C0BE   E432D0            LDM    TM0,#032H      ;TIMER0 STOP
258 C0C1   9108              CLR1   IRTFLAG        ;REPEAT FLAG
259 C0C3   6F                RET
260                     ;
261                     ;=========================================================
262                     ;           DELAY  ROUTINE
263                     ;=========================================================
264                     ;
265 C0C4   3E14          DELAY: LDY    #20
266 C0C6   7BFE              DBNE   Y,$
267 C0C8   6F                RET
268                     ;
269                     ;=========================================================
270                     ;           KEY  SCAN  ROUTINE
271                     ;=========================================================
272                     ;
273 C0C9   FF            KSCN:  NOP
274 C0CA   6F                RET
275                     ;
276                           END
                                                  -- 0 Error(s) --
                              --- Total Machine Code : 231 Bytes --
```

2-7. RC-5 (SAA3010)

2-7-1. Overview

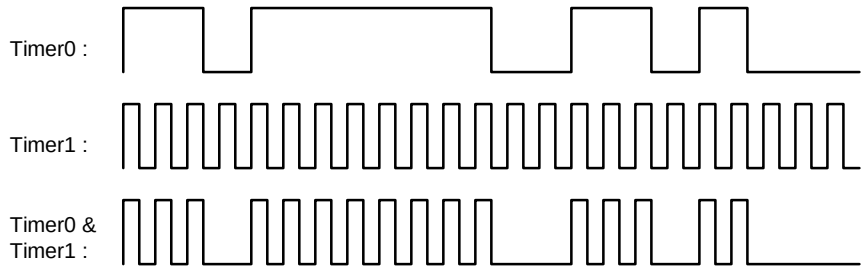
1) This program is example for RC-5
2) It shows the method of making flash carrier waveform used by Timer0 and Timer1
3) Waveform is generated by single mode and modulo-N mode combination

2-7-2. RAM Description

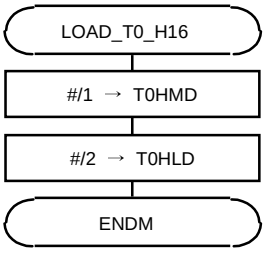
Label	Address	Description
NEWKEY	$03H	Valid Key Data Come From Key Scan Routine
KEYDATA	$07H	OLD Key Data
RPT	2, $08H	Repeat Bit ´L´
FST	3, $08H	Bit First Check Flag
BIT_CHECK	4, $08H	Bit Check Flag
RC5FLAG	5, $08H	
COUNT	$0AH	Bit Count
BUFFER	$0BH	Tx System Data Buffer
BUFFER1	$0CH	Tx Control Data Buffer

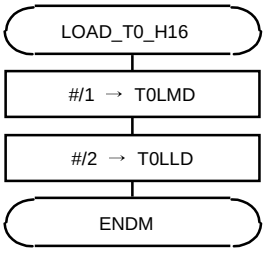
2-7-3. Module explanation

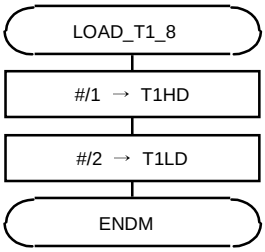
1) Timer0 is used to generate remote output signal
2) Timer1 makes carrier frequency
3) Timer0 : Single interrupt every counter overflow
4) Timer1 : Modulo-N interrupt every counter overflow

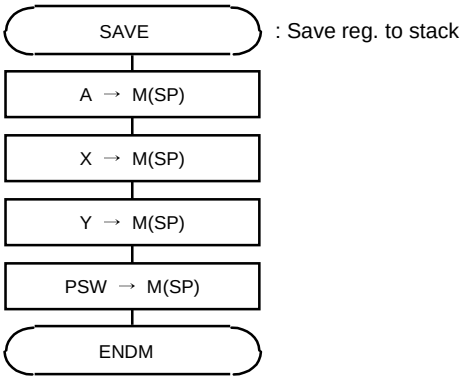


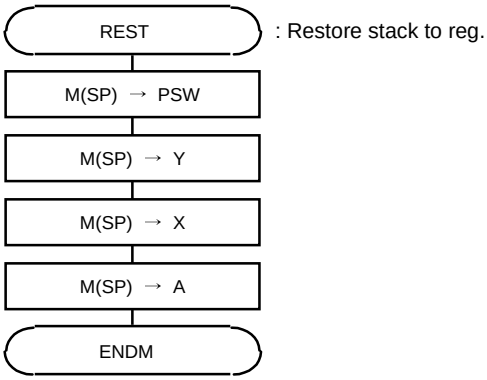
2-7-4. Flow Chart

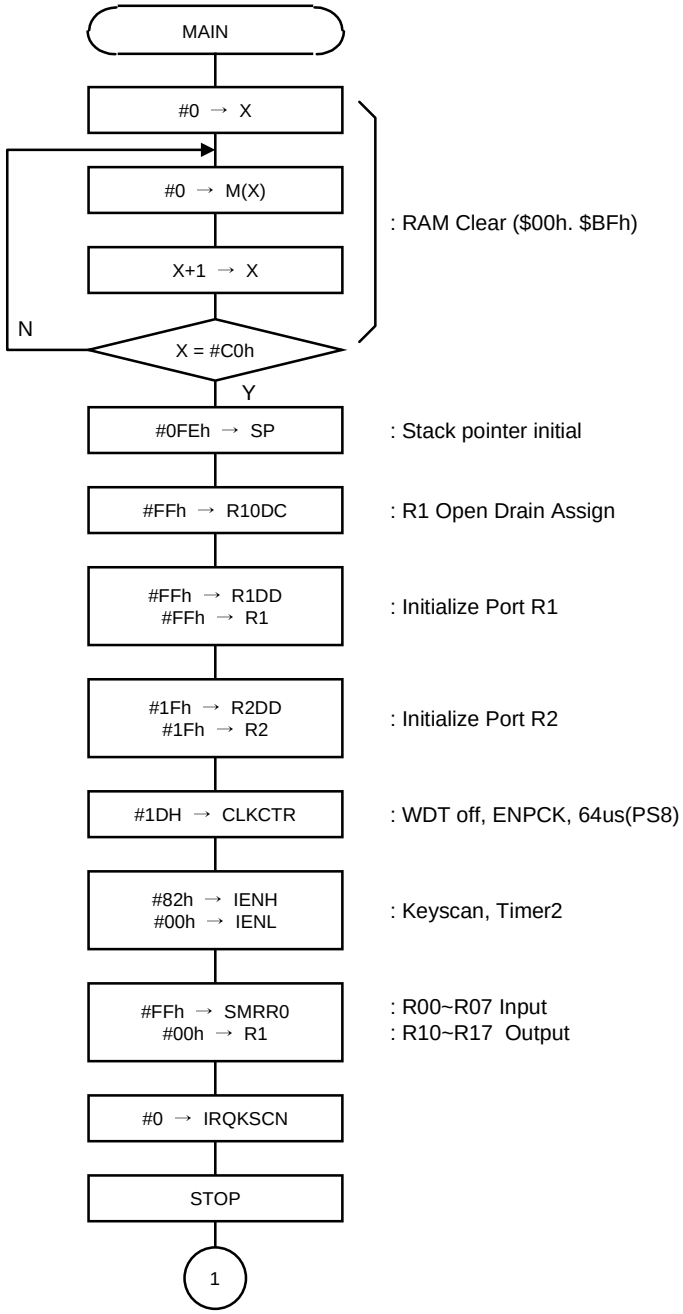


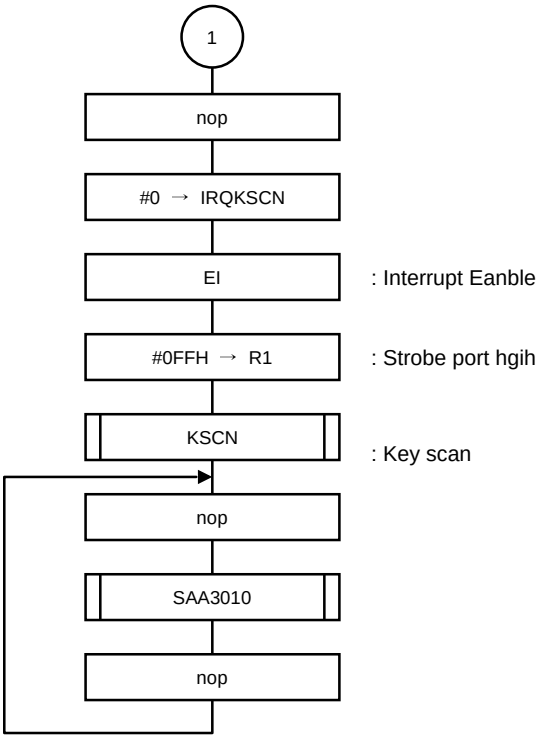


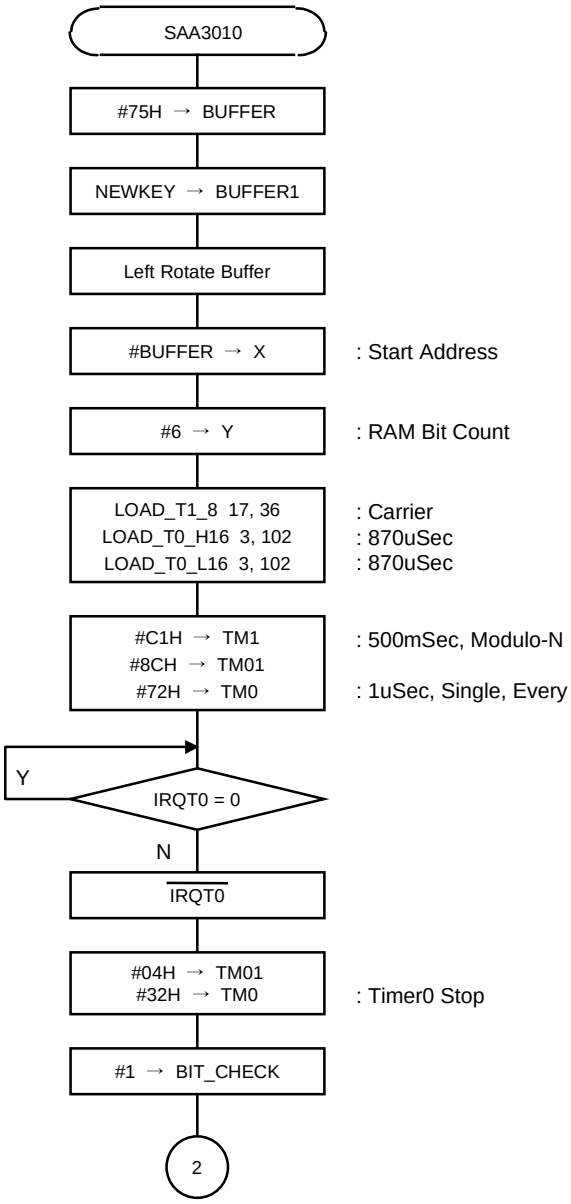


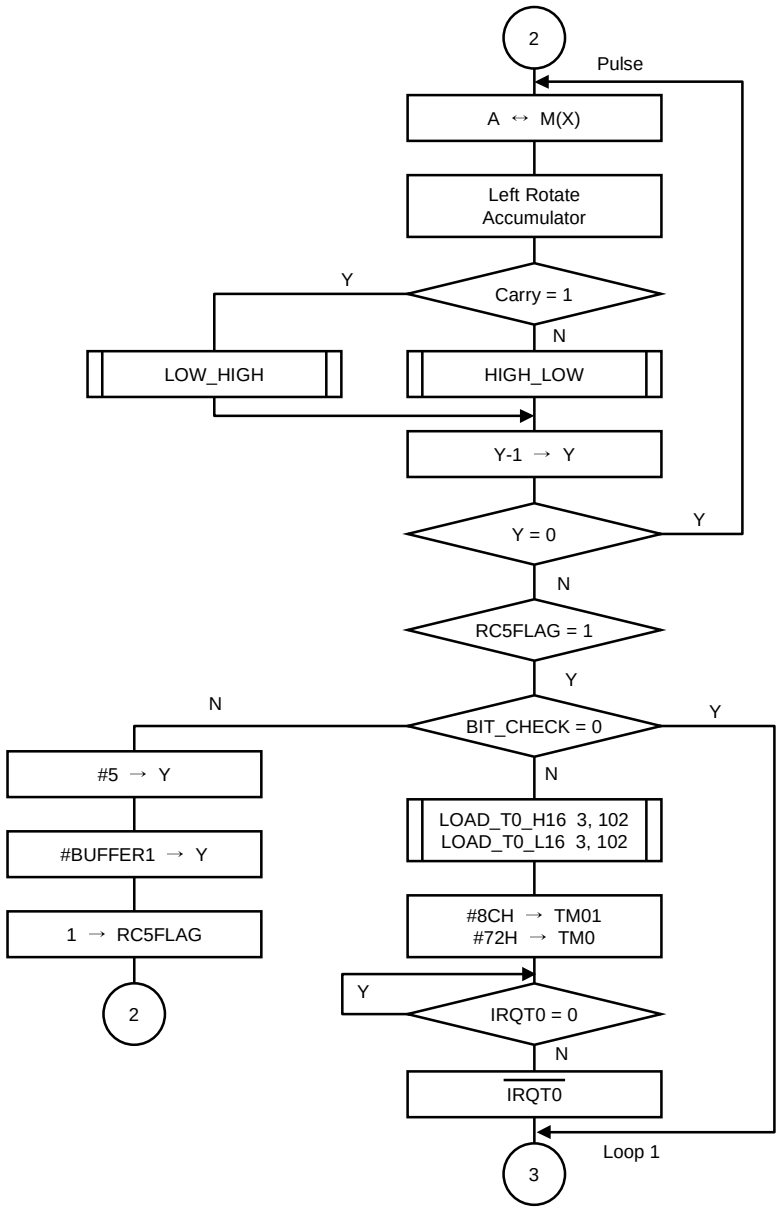


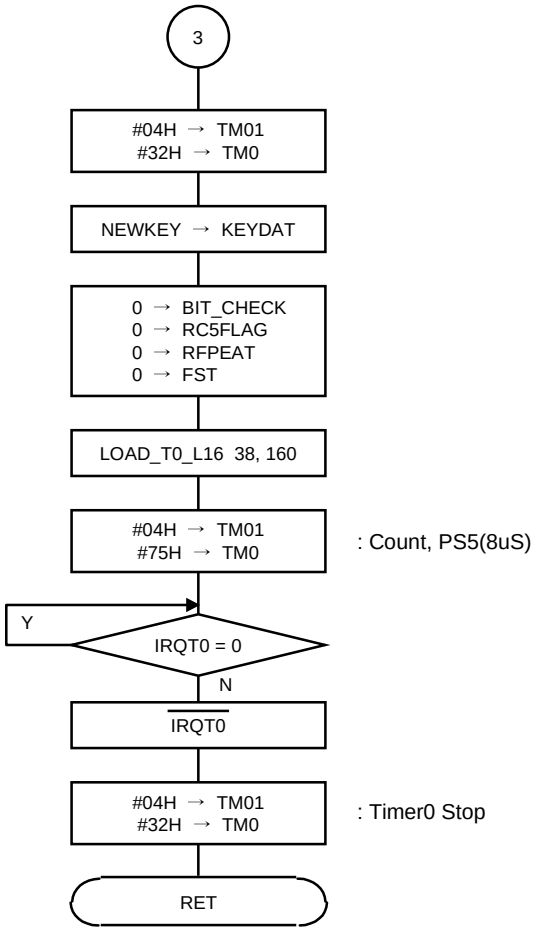


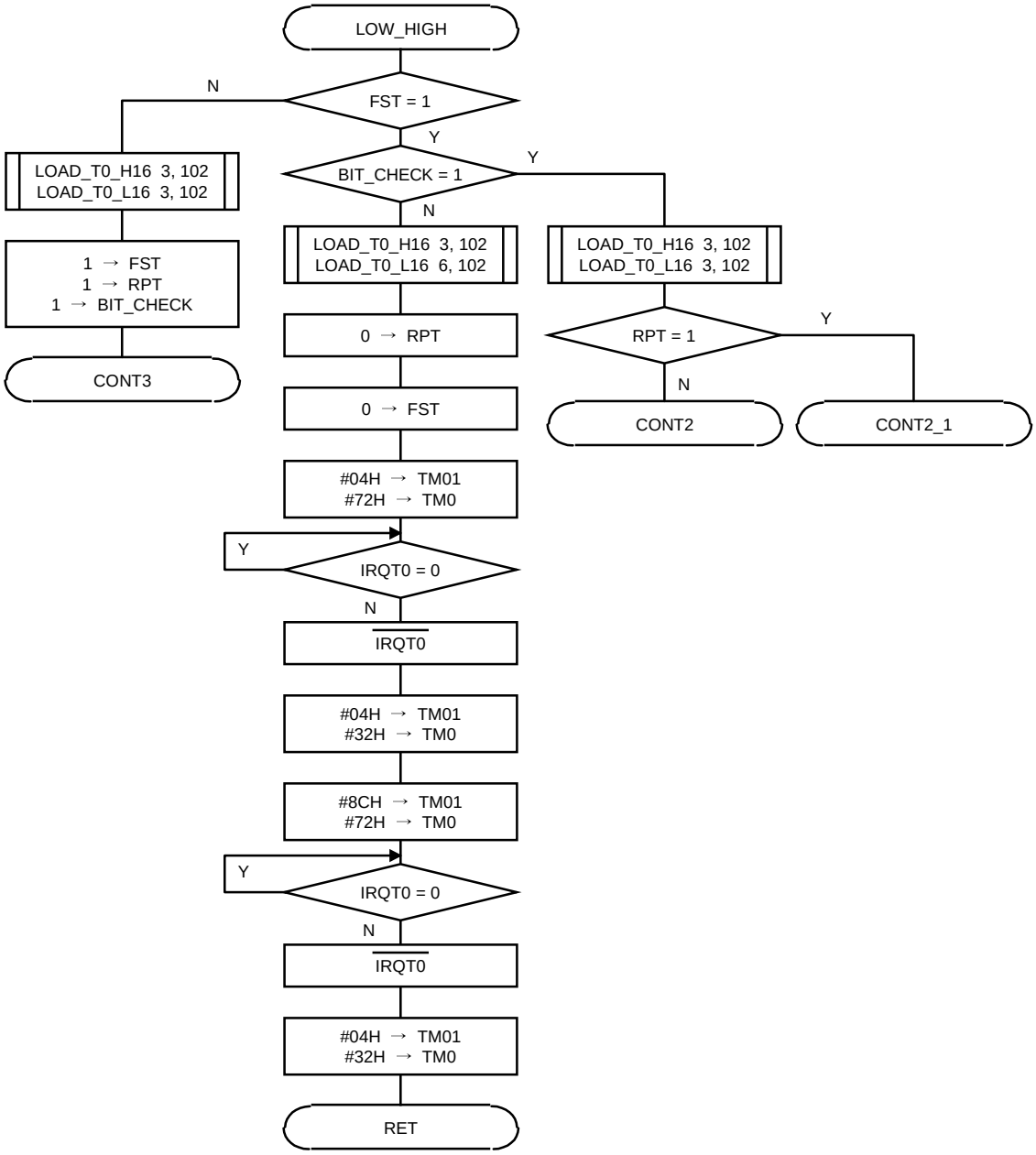

MAIN
#0 → X
#0 → M(X)
X+1 → X
N
X = #C0h
Y
: RAM Clear ($00h. $BFh)
#0FEh → SP
: Stack pointer initial
#FFh → R10DC
: R1 Open Drain Assign
#FFh → R1DD
#FFh → R1
: Initialize Port R1
#1Fh → R2DD
#1Fh → R2
: Initialize Port R2
#1DH → CLKCTR
: WDT off, ENPCK, 64us(PS8)
#82h → IENH
#00h → IENL
: Keyscan, Timer2
#FFh → SMRR0
#00h → R1
: R00~R07 Input
: R10~R17 Output
#0 → IRQKSCN
STOP
1

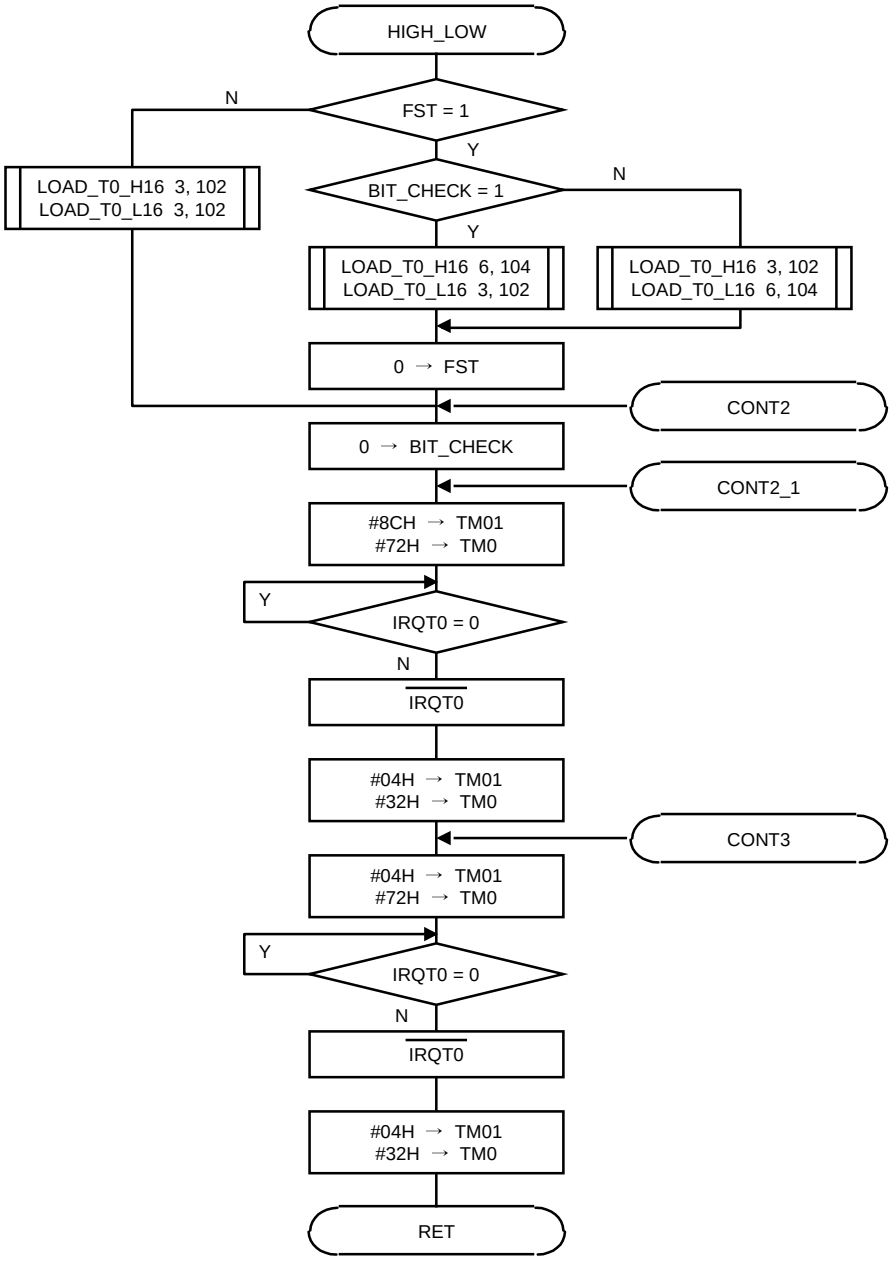

1
nop
#0 → IRQKSCN
EI
: Interrupt Eanble
#0FFH → R1
: Strobe port hgih
KSCN
: Key scan
nop
SAA3010
nop


SAA3010
#75H → BUFFER
NEWKEY → BUFFER1
Left Rotate Buffer
#BUFFER → X
: Start Address
#6 → Y
: RAM Bit Count
LOAD_T1_8 17, 36
LOAD_T0_H16 3, 102
LOAD_T0_L16 3, 102
: Carrier
: 870uSec
: 870uSec
#C1H → TM1
#8CH → TM01
#72H → TM0
: 500mSec, Modulo-N
: 1uSec, Single, Every
Y
IRQT0 = 0
N
IRQT0
#04H → TM01
#32H → TM0
: Timer0 Stop
#1 → BIT_CHECK
2


2
Pulse
A ↔ M(X)
Left Rotate
Accumulator
Y
Carry = 1
N
LOW_HIGH
HIGH_LOW
Y-1 → Y
Y
Y = 0
N
RC5FLAG = 1
Y
N
BIT_CHECK = 0
Y
#5 → Y
N
LOAD_T0_H16 3, 102
LOAD_T0_L16 3, 102
#BUFFER1 → Y
#8CH → TM01
#72H → TM0
1 → RC5FLAG
Y
IRQT0 = 0
2
N
IRQT0
Loop 1
3


3
#04H → TM01
#32H → TM0
NEWKEY → KEYDAT
0 → BIT_CHECK
0 → RC5FLAG
0 → RFPEAT
0 → FST
LOAD_T0_L16 38, 160
#04H → TM01
#75H → TM0
: Count, PS5(8uS)
Y
IRQT0 = 0
N
IRQT0
#04H → TM01
#32H → TM0
: Timer0 Stop
RET


LOW_HIGH
FST = 1
N
Y
BIT_CHECK = 1
Y
N
LOAD_T0_H16 3, 102
LOAD_T0_L16 3, 102
1 → FST
1 → RPT
1 → BIT_CHECK
CONT3
LOAD_T0_H16 3, 102
LOAD_T0_L16 6, 102
0 → RPT
0 → FST
#04H → TM01
#72H → TM0
Y
IRQT0 = 0
N
IRQT0
#04H → TM01
#32H → TM0
#8CH → TM01
#72H → TM0
Y
IRQT0 = 0
N
IRQT0
#04H → TM01
#32H → TM0
RET
LOAD_T0_H16 3, 102
LOAD_T0_L16 3, 102
RPT = 1
Y
N
CONT2
CONT2_1


HIGH_LOW
FST = 1
N
Y
LOAD_T0_H16 3, 102
LOAD_T0_L16 3, 102
BIT_CHECK = 1
N
Y
LOAD_T0_H16 6, 104
LOAD_T0_L16 3, 102
LOAD_T0_H16 3, 102
LOAD_T0_L16 6, 104
0 → FST
CONT2
0 → BIT_CHECK
CONT2_1
#8CH → TM01
#72H → TM0
Y
IRQT0 = 0
N
IRQT0
#04H → TM01
#32H → TM0
CONT3
#04H → TM01
#72H → TM0
Y
IRQT0 = 0
N
IRQT0
#04H → TM01
#32H → TM0
RET

```
GMS8xxxx Cross Assembler V1.55, By HYNIX Semiconductor, Inc.1996/01/16 16:06:47 (PAGE 1)
1                 NOLIST
95              ;============================================================
96              ;
97              ;             RC-5(SAA3010)  TX  PROGRAM
98              ;
99              ;============================================================
100             ;             RAM  ALLOCATION
101             ;============================================================
102             ;
103             NEWKEY      EQU     03H         ;NEW KEY NUMBER
104             KEYDAT      EQU     07H         ;KEY DATA(ASCII)
105             RPT         EQU     2,08H       ;REPEAT BIT "1"
106             FST         EQU     3,08H       ;RC-5 BIT FIRST CHECK FLAG
107             BIT_CHECK   EQU     4,08H       ;RC-5 BIT CHECK FLAG
108             RC5FLAG     EQU     5,08H       ;RC-5 FLAG
109             COUNT       EQU     0AH         ;BIT COUNT
110             BUFFER      EQU     0BH         ;TX DATA  BUFFER
111             BUFFER1     EQU     0CH
112             ;
113             ;============================================================
114             ;             MACRO  DEFINITION
115             ;============================================================
116             LOAD_T0_H16 MACRO           ;LOAD HIGH_DATA FOR TIMER0
117                 LDM       T0HMD,#\1
118                 LDM       T0HLD,#\2
119                 ENDM
120             ;
121             LOAD_T0_L16 MACRO           ;LOAD LOW_DATA FOR TIMER0
122                 LDM       T0LMD,#\1
123                 LDM       T0LLD,#\2
124                 ENDM
125             ;
126             LOAD_T1_8 MACRO             ;LOAD 8BIT DATA FOR TIMER1
127                 LDM       T1HD,#\1
128                 LDM       T1LD,#\2
129                 ENDM
130             ;
131             SAVE    MACRO               ;REGISTER SAVE
132                 PUSH      A
133                 PUSH      X
134                 PUSH      Y
135                 PUSH      PSW
136                 ENDM
137             ;
138             REST    MACRO               ;REGISTER RESTORE
139                 POP       PSW
```

```
GMS8xxxx Cross Assembler V1.55, By HYNIX Semiconductor, Inc.1996/01/16 16:06:47 (PAGE 2)
140                     POP    Y
141                     POP    X
142                     POP    A
143                     ENDM
144                 ;
145<N>              ;=============================================================
146                 ;           INTERRUPT  VECTOR  TABLE
147<N>              ;=============================================================
148                 ;
149                 ORG    0FFE4H
150                 ;
151 FFE4   FF       NOTUSE:  NOP
152 FFE5   7F            RETI
153                 ;
154 FFE6   E4FF          DW     NOTUSE          ;BASIC INTERVAL TIMER
155 FFE8   E4FF          DW     NOTUSE          ;WATCH DOG TIMER
156 FFEA   E4FF          DW     NOTUSE          ;A/D CONVERTER
157 FFEC   E4FF          DW     NOTUSE          ;TIMER-3
158 FFEE   E4FF          DW     NOTUSE          ;TIMER-2
159 FFF0   E4FF          DW     NOTUSE          ;TIMER-1
160 FFF2   E4FF          DW     NOTUSE          ;TIMER-0
161 FFF4   E4FF          DW     NOTUSE          ;INT 3
162 FFF6   E4FF          DW     NOTUSE          ;INT 2
163 FFF8   E4FF          DW     NOTUSE          ;INT 1
164 FFFA   E4FF          DW     NOTUSE          ;KEY SCAN
165 FFFC   E4FF          DW     NOTUSE
166 FFFE   00C0          DW     MAIN            ;RESET
167                 ;
168<N>              ;=============================================================
169                 ;           MAIN  PROGRAM
170<N>              ;=============================================================
171                 ;
172                       ORG    0C000H
173 C000 1E00       MAIN:  LDX    #0
174 C002 C400             LDA    #0              ;RAM CLEAR(!0000H-!00BFH)
175 C004 FB          CLR:  STA    {X}+
176 C005 5EC0              CMPX   #0C0H
177 C007 70FB              BNE    CLR
178 C009 1EFE              LDX    #0FEH           ;STACK POINTER INITIAL
179 C00B 8E                TXSP
180                 ;
181 C00C E4FFDE            LDM    R1ODC,#0FFH     ;R1 OPEN DRAIN ASSIGN REG.
182 C00F E4FFC3            LDM    R1DD,#0FFH      ;DATA DIRECTION REG.
183 C012 E4FFC2            LDM    R1,#0FFH        ;R1 DATA REG.
184 C015 E41FC5            LDM    R2DD,#1FH       ;DATA DIRECTION REG.
185 C018 E41FC4            LDM    R2,#1FH         ;R2 DATA REG. OUTPUT
```

```
GMS8xxxx Cross Assembler V1.55, By HYNIX Semiconductor, Inc.1996/01/16 16:06:47 (PAGE 3)
186 C01B   E41DC7          LDM    CLKCTR,#1DH       ;WDT OFF, ENPCK, 64uS(PS8)
187 C01E   E480CE          LDM    IENH,#80H         ;KEYSCAN
188 C021   E400CC          LDM    IENL,#00H         ;WATCH DOG TIMER
189 C024   E4FFDC          LDM    SMRR0,#0FFH       ;R00~7 INPUT
190 C027   E400C2          LDM    R1,#00H           ;R10~7 STROBE ENABLE(OUTPUT)
191 C02A   F1CF            CLR1   IRQKSCN
192 C02C   00              STOP
193                    ;
194 C02D   FF              NOP
195 C02E   F1CF            CLR1   IRQKSCN
196 C030   E0              EI
197 C031   E4FFC2          LDM    R1,#0FFH          ;STROBE PORT HIGH
198 C034   3B96C1          CALL   KSCN              ;TEST IF KEY PRESSED
199 C037   FF      TX_LOOP: NOP
200 C038   3B3EC0          CALL   SAA3010
201 C03B   FF              NOP
202 C03C   2FF9            BRA    TX_LOOP
203                    ;
204<N>                  ;============================================================
205                    ;            RC-5(SAA3010)  TX  ROUTINE
206<N>                  ;============================================================
207                    ;
208 C03E   E4750B      SAA3010: LDM    BUFFER,#75H      ;
209 C041   C503            LDA    NEWKEY
210 C043   E50C            STA    BUFFER1
211                    [BUFFER]=[BUFFER]<<1
212 C045   C50B  @         lda    BUFFER
213 C047   08    @         asl    A
214 C048   E50B  @         sta    BUFFER
215                    [BUFFER1]=[BUFFER1]<<2
216 C04A   C50C  @       l da     BUFFER1
217 C04C   08    @         asl    A
218 C04D   08    @         asl    A
219 C04E   E50C  @         sta    BUFFER1
220 C050   1E0B            LDX    #BUFFER           ;START ADDRESS
221 C052   3E06            LDY    #6                ;RAM BIT COUNT
222                    ;
223                    HEAD: LOAD_T1_8 17,36        ;CARRIER HI=500nS x 17= 8.5uS
224 C054   E411D7 @        LDM    T1HD,#17
225 C057   E424D8 @        LDM    T1LD,#36
226                    LOAD_T0_H16 3,102            ;870uS
227 C05A   E403D3 @        LDM    T0HMD,#3
228 C05D   E466D4 @        LDM    T0HLD,#102
229                    LOAD_T0_L16 3,102            ;870uS
230 C060   E403D5 @        LDM    T0LMD,#3
231 C063   E466D6 @        LDM    T0LLD,#102
```

```
GMS8xxxx Cross Assembler V1.55, By HYNIX Semiconductor, Inc.1996/01/16 16:06:47 (PAGE 4)
232 C066   E4C1D1          LDM    TM1,#0C1H       ;500nS, MODULO
233 C069   E48CDA          LDM    TM01,#08CH      ;T0/1 HIGH T0 AND T1
234 C06C   E472D0          LDM    TM0,#072H       ;1uS, SINGLE, EVERY
235 C06F   73CFFD          BBC    IRQT0,$
236 C072   4BCF60          NOT1   IRQT0
237 C075   E404DA          LDM    TM01,#04H
238 C078   E432D0          LDM    TM0,#32H        ;TIMER0 STOP
239 C07B   8108            SET1   BIT_CHECK
240                    ;
241 C07D   BB          PULSE:  XMA    {X}
242 C07E   28                 ROL    A
243 C07F   D005               BCS    HIGH
244 C081   3B3FC1             CALL   HIGH_LOW      ;T0/1 HIGH T0 AND T1
245 C084   2F03               BRA    LOW
246                    ;
247 C086   3BDCC0  HIGH:   CALL   LOW_HIGH    ;T0/1 INITIAL VALUE LOW
248 C089   BB              LOW:    XMA    {X}
249 C08A   BE                 DEC    Y
250 C08B   10F0               BPL    PULSE
251 C08D   A30808             BBS    RC5FLAG,LOOP
252 C090   3E05               LDY    #5              ;RAM BIT COUNT
253 C092   1E0C               LDX    #BUFFER1        ;BUFFER INCREMENT
254 C094   A108               SET1   RC5FLAG
255 C096   2FE5               BRA    PULSE
256                    ;
257 C098   930818      LOOP:   BBC    BIT_CHECK,LOOP1
258                    LOAD_T0_H16 3,102           ;870uS
259 C09B   E403D3 @           LDM    T0HMD,#3
260 C09E   E466D4 @           LDM    T0HLD,#102
261                    LOAD_T0_L16 3,102           ;870uS
262 C0A1   E403D5 @           LDM    T0LMD,#3
263 C0A4   E466D6 @           LDM    T0LLD,#102
264 C0A7   E48CDA             LDM    TM01,#08CH      ;T0/1 HIGH T0 AND T1
265 C0AA   E472D0             LDM    TM0,#072H       ;1uS, SINGLE, EVERY
266 C0AD   73CFFD             BBC    IRQT0,$
267 C0B0   4BCF60             NOT1   IRQT0
268 C0B3   E404DA  LOOP1:  LDM    TM01,#04H
269 C0B6   E432D0             LDM    TM0,#32H        ;TIMER0 STOP
270 C0B9   C503               LDA    NEWKEY
271 C0BB   E507               STA    KEYDAT
272 C0BD   9108               CLR1   BIT_CHECK
273 C0BF   B108               CLR1   RC5FLAG
274 C0C1   7108               CLR1   FST
275                    ;
276                    LOAD_T0_L16 38,160
277 C0C3   E426D5 @           LDM    T0LMD,#38
```

```
GMS8xxxx Cross Assembler V1.55, By HYNIX Semiconductor, Inc.1996/01/16 16:06:47 (PAGE 5)
278 C0C6   E4A0D6 @          LDM    T0LLD,#160
279 C0C9   E404DA            LDM    TM01,#04H
280 C0CC   E475D0            LDM    TM0,#75H        ;COUNT, PS5(8uS)
281 C0CF   73CFFD            BBC    IRQT0,$
282 C0D2   4BCF60            NOT1   IRQT0
283 C0D5   E404DA            LDM    TM01,#04H
284 C0D8   E432D0            LDM    TM0,#32H        ;TIMER0 STOP
285 C0DB   6F                RET
286                     ;
287 C0DC   630815       LOW_HIGH: BBS    FST,LOW1   ;BIT  "1"
288                     LOAD_T0_H16 3,102            ;870uS
289 C0DF   E403D3 @          LDM    T0HMD,#3
290 C0E2   E466D4 @          LDM    T0HLD,#102
291                     LOAD_T0_L16 3,102            ;870uS
292 C0E5   E403D5 @          LDM    T0LMD,#3
293 C0E8   E466D6 @          LDM    T0LLD,#102
294 C0EB   6108              SET1   FST
295 C0ED   4108              SET1   RPT
296 C0EF   8108              SET1   BIT_CHECK
297 C0F1   1B83C1            JMP    CONT3
298 C0F4   830810   LOW1:    BBS    BIT_CHECK,LOW2
299                     LOAD_T0_H16 3,102            ;870uS
300 C0F7   E403D3 @          LDM    T0HMD,#3
301 C0FA   E466D4 @          LDM    T0HLD,#102
302                     LOAD_T0_L16 6,104            ;1740uS
303 C0FD   E406D5 @          LDM    T0LMD,#6
304 C100   E468D6 @          LDM    T0LLD,#104
305 C103   5108              CLR1   RPT
306 C105   2F11              BRA    LOW3
307                     LOW2: LOAD_T0_H16 3,102      ;870uS
308 C107   E403D3 @          LDM    T0HMD,#3
309 C10A   E466D4 @          LDM    T0HLD,#102
310                     LOAD_T0_L16 3,102            ;870uS
311 C10D   E403D5 @          LDM    T0LMD,#3
312 C110   E466D6 @          LDM    T0LLD,#102
313 C113   43085B            BBS    RPT,CONT2_1    ;REPEAT BIT "1"
314 C116   2F57              BRA    CONT2
315 C118   7108         LOW3:   CLR1   FST
316 C11A   E404DA            LDM    TM01,#04H       ;T0/1 HIGH T0 AND T1
317 C11D   E472D0            LDM    TM0,#072H       ;1uS, SINGLE, EVERY
318 C120   73CFFD            BBC    IRQT0,$
319 C123   4BCF60            NOT1   IRQT0
320 C126   E404DA            LDM    TM01,#04H
321 C129   E432D0            LDM    TM0,#32H        ;TIMER0 STOP
322 C12C   E48CDA            LDM    TM01,#8CH       ;T0/1 HIGH T0 AND T1
323 C12F   E472D0            LDM    TM0,#072H       ;1uS, SINGLE, EVERY
```

```
GMS8xxxx Cross Assembler V1.55, By HYNIX Semiconductor, Inc.1996/01/16 16:06:47 (PAGE 6)
324 C132   73CFFD          BBC    IRQT0,$
325 C135   4BCF60          NOT1   IRQT0
326 C138   E404DA          LDM    TM01,#04H
327 C13B   E432D0          LDM    TM0,#32H            ;TIMER0 STOP
328 C13E   6F              RET
329                ;
330 C13F   63080E     HIGH_LOW: BBS    FST,BITT        ;BIT  "0"
331                LOAD_T0_H16 3,102                   ;870uS
332 C142   E403D3 @        LDM    T0HMD,#3
333 C145   E466D4 @        LDM    T0HLD,#102
334                LOAD_T0_L16 3,102                   ;870uS
335 C148   E403D5 @        LDM    T0LMD,#3
336 C14B   E466D6 @        LDM    T0LLD,#102
337 C14E   2F1F            BRA    CONT2
338 C150   83080E     BITT:   BBS    BIT_CHECK,CONT
339                LOAD_T0_H16 3,102                   ;870uS
340 C153   E403D3 @        LDM    T0HMD,#3
341 C156   E466D4 @        LDM    T0HLD,#102
342                LOAD_T0_L16 6,104                   ;1740uS
343 C159   E406D5 @        LDM    T0LMD,#6
344 C15C   E468D6 @        LDM    T0LLD,#104
345 C15F   2F0C            BRA    CONT1
346                CONT: LOAD_T0_H16 6,104             ;1740uS
347 C161   E406D3 @        LDM    T0HMD,#6
348 C164   E468D4 @        LDM    T0HLD,#104
349                LOAD_T0_L16 3,102          ;870uS
350 C167   E403D5 @        LDM    T0LMD,#3
351 C16A   E466D6 @        LDM    T0LLD,#102
352 C16D   7108        CONT1:  CLR1   FST
353 C16F   9108        CONT2:  CLR1   BIT_CHECK
354 C171   E48CDA      CONT2_1: LDM    TM01,#08CH      ;T0/1 HIGH T0 AND T1
355 C174   E472D0          LDM    TM0,#072H           ;1uS, SINGLE, EVERY
356 C177   73CFFD          BBC    IRQT0,$
357 C17A   4BCF60          NOT1   IRQT0
358 C17D   E404DA          LDM    TM01,#04H
359 C180   E432D0          LDM    TM0,#32H            ;TIMER0 STOP
360 C183   E404DA      CONT3:  LDM    TM01,#04H       ;T0/1 HIGH T0 AND T1
361 C186   E472D0          LDM    TM0,#072H           ;1uS, SINGLE, EVERY
362 C189   73CFFD          BBC    IRQT0,$
363 C18C   4BCF60          NOT1   IRQT0
364 C18F   E404DA          LDM    TM01,#04H
365 C192   E432D0          LDM    TM0,#32H            ;TIMER0 STOP
366 C195   6F              RET
367                ;
368<N>             ;=======================================================
369                ;           KEY  SCAN  ROUTINE
```

```
GMS8xxxx Cross Assembler V1.55, By HYNIX Semiconductor, Inc.1996/01/16 16:06:47 (PAGE 7)
370;============================================================
371 C196   FF          KSCN:   NOP
372 C197   6F                  RET
373                    ;
374                            END

                               -- 0 Error(s) --

                       --- Total Machine Code : 436 Bytes --
```

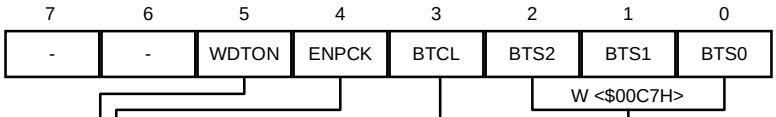
APPENDIX.A

PERIPHERAL REGISTERS MEMORY MAP

ADDRESS	FUNCTION REGISTERS	R/W	SYMBOL
00C0H	PORT R0 DATA REG.	R/W	R0
00C1H	PORT R0 DATA DIRECTION REG.	W	R0DD
00C2H	PORT R1 DATA REG.	R/W	R1
00C3H	PORT R1 DATA DIRECTION REG.	W	R1DD
00C4H	PORT R2 DATA REG.	R/W	R2
00C5H	PORT R0 DATA DIRECTION REG.	W	R2DD
00C6H	TEST MODE REG.	W	RTMR
00C7H	CLOCK CONTROL REG.	W	CKCTLR
	BASIC INTERVAL REG.	R	BITR
00C8H	WATCH DOG TIMER REG.	W	WDTR
00C9H	PORT R1 MODE REG.	W	PMR1
00CAH	INT. MODE REG..	R/W	IMOD
00CBH	EXT. INT. EDGE SELECTION	W	IEDS
00CCH	INT. ENABLE REG. LOW	R/W	IENL
00CDH	INT. REQUEST FLAG REG. LOW	R/W	IRQL
00CEH	INT. ENABLE REG. HIGH	R/W	IENH
00CFH	INT. REQUEST FLAG REG. LOW	R/W	IRQH
00D0H	TIMER0 (16bit) MODE REG.	R/W	TM0
00D1H	TIMER1 (8bit) MODE REG.	R/W	TM1
00D2H	TIMER2 (8bit) MODE REG.	R/W	TM2
00D3H	TIMER0 HIGH-MSB DATA REG.	W	T0HMD
00D4H	TIMER0 HIGH-LSB DATA REG.	W	T0HLD
00D5H	TIMER0 LOW-MSB DATA REG.	W	T0MLD
	TIMER0 LOW-MSB COUNT REG.	R	
00D6H	TIMER0 LOW-LSB DATA REG.	W	T0LLD
	TIMER0 LOW-LSB COUNT REG.	R	
00D7H	TIMER1 HIGH DATA REG.	W	T1HD
00D8H	TIMER1 LOW DATA REG.	W	T1LD
	TIMER1 LOW COUNT REG.	R	
00D9H	TIMER2 DATA REG.	W	T2DR
	TIMER2 COUNT REG.	R	
00DAH	TIMER0/TIMR1 MODE REG.	R/W	TM01
00DBH	Reserved		
00DCH	STANDBY MODE RELEASE REG0	W	SMRR0
00DDH	STANDBY MODE RELEASE REG1	W	SMRR1
00DEH	PORT R1 OPEN DRAIN ASSIGN REG.	W	R1ODC

APPENDIX.B

1) CKCTLR (Clock Control Register)



BTS2	BTS1	BTS0	B.I.T Input clock	INT. interval time
0	0	0	PS3 (2us)	512us
0	0	1	PS4 (4us)	1,024us
0	1	0	PS5 (8us)	2,048us
0	1	1	PS6 (16us)	4,096us
1	0	0	PS7 (32us)	8,192us
1	0	1	PS8 (64us)	16,384us
1	1	0	PS9 (128us)	32,768s
1	1	1	PS10 (256us)	65,536us

BTCL	B.I.T Operation
0	bit free run
1	bit clear automaticall cleared, after 1 cycle

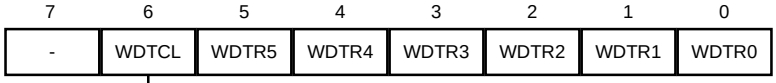
ENPCK	Peripheral Clock
0	stop
1	provide

WDTON	Watch Dog Timer Function Control
0	6 bit timer
1	Watch Dog Timer

◆ BITR(Basic Interval Timer Register)

W <$00C7H>

2) WDTR (Watch Dog Timer Register)

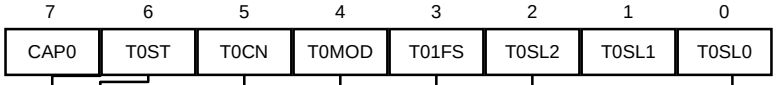


W <$00C8H>

Determine Interval of IFWDT
Interval of IFWDT = (Value of WDTR) * (Interval of IFBIT)

WDTCL	Watch Dog Timer Operation
0	Free run
1	Automatically cleared, after 1 machine cycle

3) TM0 (Timer0 Mode Register)



T0SL2	T0SL1	T1SL0	Input clock Sel.	Notes
0	0	0	PS0 (2us)	
0	0	1	PS1 (4us)	
0	1	0	PS2 (8us)	
0	1	1	PS3 (16us)	
1	0	0	PS4 (32us)	
1	0	1	PS5 (64us)	
1	1	0	PS11 (128us)	
1	1	1	$\overline{EC}$	Event Counter

T0IFS	Timer0 Interrupt Sel.
0	Interrupt Every Counter Overflow
1	Interrupt Every 2nd Counter Overflow

T0MOD	Timer0 Single / Modulo-N Sel.
0	Modulo-N
1	Single Mode

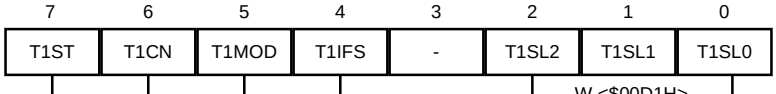
T0CN	Timer0 Counter Continuation / Pause Control
0	Count Pause
1	Count Continuation

T0ST	Timer0 Start/Stop control
0	Timer0 Stop
1	Timer0 Start after Clear

CAP0	Timer0 Interrupt Sel.
0	Timer/Counter
1	Input Capture

*PS1 : not supporting input capture

4) TM1 (Timer1 Mode Register)



T1SL2	T1SL1	T1SL0	Input clock Sel.
0	0	0	PS0 (250us)
0	0	1	PS1 (500us)
0	1	0	PS2 (1us)
0	1	1	PS3 (2us)
1	0	0	PS4 (32us)
1	0	1	PS5 (64us)
1	1	0	PS11 (128us)
1	1	1	PS12 (256us)

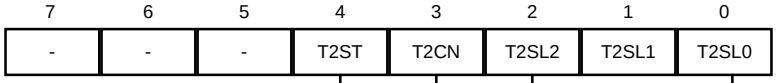
T1IFS	Timer1 Interrupt Sel.
0	Interrupt Every Counter Overflow
1	Interrupt Every 2nd Counter Overflow

T1MOD	Timer1 Single / Modulo-N Sel.
0	Modulo-N
1	Single Mode

T1CN	Timer1 Counter Continuation / Pause Control
0	Count Pause
1	Count Continuation

T1ST	Timer1 Start/Stop control
0	Timer1 Stop
1	Timer1 Start after Clear

5) TM1 (Timer1 Mode Register)

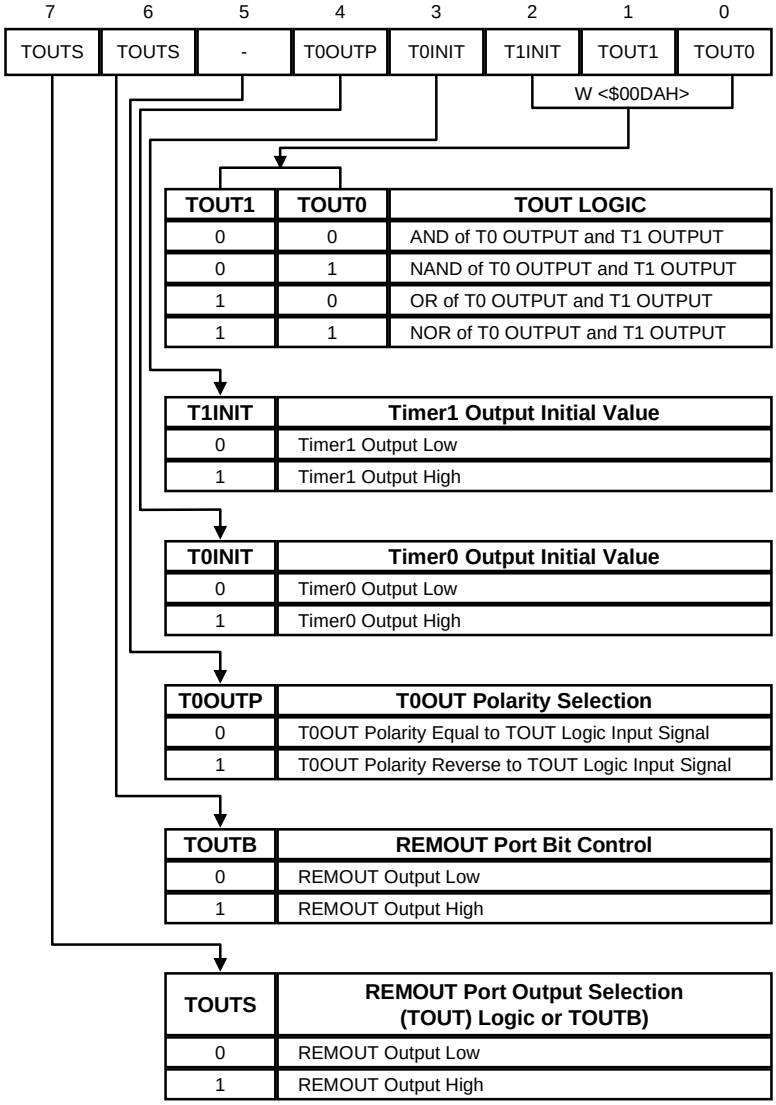


T2SL2	T2SL1	T2SL0	Input clock Sel.
0	0	0	PS5 (8us)
0	0	1	PS6 (16us)
0	1	0	PS7 (32us)
0	1	1	PS8 (64us)
1	0	0	PS9 (128us)
1	0	1	PS10 (256us)
1	1	0	PS11 (513us)
1	1	1	PS12 (1024us)

T2CN	Timer2 Counter Continuation/Pause Control
0	Count Pause
1	Count Continuation

T2ST	Timer2 Start/Stop Control
0	Timer2 Stop
1	Timer 2 Start after Clear

6) TM01 (Timer0/1 Mode Register)



TOUT1	TOUT0	TOUT LOGIC
0	0	AND of T0 OUTPUT and T1 OUTPUT
0	1	NAND of T0 OUTPUT and T1 OUTPUT
1	0	OR of T0 OUTPUT and T1 OUTPUT
1	1	NOR of T0 OUTPUT and T1 OUTPUT

T1INIT	Timer1 Output Initial Value
0	Timer1 Output Low
1	Timer1 Output High

T0INIT	Timer0 Output Initial Value
0	Timer0 Output Low
1	Timer0 Output High

T0OUTP	T0OUT Polarity Selection
0	T0OUT Polarity Equal to TOUT Logic Input Signal
1	T0OUT Polarity Reverse to TOUT Logic Input Signal

TOUTB	REMOUT Port Bit Control
0	REMOUT Output Low
1	REMOUT Output High

TOUTS	REMOUT Port Output Selection (TOUT) Logic or TOUTB)
0	REMOUT Output Low
1	REMOUT Output High

7) PMR1 (Port Mode Register 1)

7	6	5	4	3	2	1	0
T0S	T1S	T2S	ECS	-	INT2S	INT1S	-

W <$00C9H>

PMR1		PORT Sel.	Remarks
T0S	0	R17 (I/O)	-
	1	T0 (Output)	Output Port of Timer0
T1S	0	R16 (I/O)	-
	1	T1 (Output)	Output Port of Timer1
T2S	0	R15 (I/O)	-
	1	T2 (Output)	Output Port of Timer2
ECS	0	R14 (I/O)	-
	1	EC (Input)	Input Port of Timer0 Event
-	-	-	-
	-	-	-
INT2S	0	R12 (I/O)	-
	1	INT2 (Input)	Input Port of Timer0 Input Capture
INT1S	0	R11 (I/O)	-
	1	INT1 (Input)	-
-	-	-	-
	-	-	-

8) IEDS (External Interrupt Signal Edge Selection Register)

7	6	5	4	3	2	1	0
-	-	IED2H	IED2L	IED1H	IED1L	-	-

W <$00CBH>

IED*H	IED*L	Int.
0	0	-
0	1	Falling Edge Selection
1	0	Rising Edge Selection
1	1	Both Edge Selection

APPENDIX.C INSTRUCTION SET TABLE

No.	MNEMONIC		OP CODE	Words	Exec. Cycle	OPERATION	Flag MVGHIZC
1	ADC	#imm	04	2	2	A = A + op + C	N V . . H . Z C
2	ADC	dp	05	2	3	″	N V . . H . Z C
3	ADC	dp+X	06	2	4	″	N V . . H . Z C
4	ADC	!abs	07	3	4	″	N V . . H . Z C
5	ADC	!abs+Y	15	3	5	″	N V . . H . Z C
6	ADC	[dp+X]	16	2	6	″	N V . . H . Z C
7	ADC	[dp]+Y	17	2	6	″	N V . . H . Z C
8	ADC	{X}	14	1	3	″	N V . . H . Z C
9	AND	#imm	84	2	2	A = A & op	N . . . . . Z .
10	AND	dp	85	2	3	″	N . . . . . Z .
11	AND	dp+X	86	2	4	″	N . . . . . Z .
12	AND	!abs	87	3	4	″	N . . . . . Z .
13	AND	!abs+Y	95	3	5	″	N . . . . . Z .
14	AND	[dp+X]	96	2	6	″	N . . . . . Z .
15	AND	[dp]+Y	97	2	6	″	N . . . . . Z .
16	AND	{X}	94	1	3	″	N . . . . . Z .
17	ASL	A	08	1	2	op = op << 1	N . . . . . Z C
18	ASL	dp	09	2	4	″	N . . . . . Z C
19	ASL	dp+X	19	2	5	″	N . . . . . Z C
20	ASL	!abs	18	3	5	″	N . . . . . Z C
21	BBC	A.bit, rel	y2	2	4/6	if (bit = 0)	. . . . .
22	BBC	dp.bit, rel	y3	3	5/7	then branch	. . . . .
23	BBS	A.bit, rel	x2	2	4/6	if (bit = 1)	. . . . .
24	BBS	dp.bit, rel	x3	3	5/7	then branch	. . . . .
25	BCC	rel	50	2	2/4	if (C=0) branch	. . . . .
26	BCS	rel	D0	2	2/4	if (C=1) branch	. . . . .
27	BEQ	rel	F0	2	2/4	if (Z=1) branch	. . . . .
28	BIT	dp	0C	2	4	Z = A & op	M M . . . . Z .
29	BIT	!abs	1C	3	5	″	M M . . . . Z .
30	BMI	rel	90	2	2/4	if (N=1) branch	. . . . .
31	BNE	rel	70	2	2/4	if (Z=0) branch	. . . . .
32	BPL	rel	10	2	2/4	if (N=0) branch	. . . . .
33	BRA	rel	2F	2	4	Branch	. . . . .
34	BRK		0F	1	8	S/W interrupt	. . . 1 . 0 . .
35	BVC	rel	30	2	2/4	if (V=0) branch	. . . . .
36	BVS	rel	B0	2	2/4	if (V=1) branch	. . . . .
37	CLR1	dp.bit	y1	2	4	op.bit = 0	. . . . .
38	CLRA1	A.bit	2B	2	2	″	. . . . .
39	CLRC		20	1	2	C = 0	 0
40	CLRG		40	1	2	G = 0	. . 0 . . . . .
41	CLRV		80	1	2	V = 0	. 0 . . 0 . . .

APPENDIX.C

No.	MNEMONIC		OP CODE	Words	Exec. Cycle	OPERATION	Flag MVG HIZC
42	CMO	#imm	44	2	2	Compare A, op	N . . . . . Z C
43	CMP	dp	45	2	3	˝	N . . . . . Z C
44	CMP	dp+X	46	2	4	˝	N . . . . . Z C
45	CMP	!abs	47	3	4	˝	N . . . . . Z C
46	CMP	!abs+Y	55	3	5	˝	N . . . . . Z C
47	CMP	[dp+X]	56	2	6	˝	N . . . . . Z C
48	CMP	[dp]+Y	57	2	6	˝	N . . . . . Z C
49	CMP	{X}	54	1	3	˝	N . . . . . Z C
50	COM	dp	2C	2	4	dp = $\overline{dp}$	N . . . . . Z .
51	CMPX	#imm	5E	2	2	Compare X, op	N . . . . . Z C
52	CMPX	dp	6C	2	3	˝	N . . . . . Z C
53	CMPX	!abs	7C	3	4	˝	N . . . . . Z C
54	CMPY	#imm	7E	2	2	Compare Y, op	N . . . . . Z C
55	CMPY	dp	8C	2	3	˝	N . . . . . Z C
56	CMPY	!abs	9C	3	4	˝	N . . . . . Z C
57	DAA		DF	1	3	˝ Dec. adjustment (Add)	N . . . . . Z C
58	DAS		CF	1	3	Dec. adjustment (Sub)	N . . . . . Z C
59	DEC	A	A8	1	2		N . . . . . Z .
60	DEC	dp	A9	2	4	op = op -1	N . . . . . Z .
61	DEC	dp + X	B9	2	5	˝	N . . . . . Z .
62	DEC	!abs	B8	3	5	˝	N . . . . . Z .
63	DEC	X	AF	1	2	˝	N . . . . . Z .
64	DEC	Y	BE	1	2	˝	N . . . . . Z .
65	DIV		9B	1	12	˝ Q:A, R:Y ← YA/X	N V . . H . Z .
66	DI		60	1	3	I = 0	. . . . . 0 . .
67	EI		E0	1	3	I = 1	. . . . . 1 . .
68	EOR	#imm	A4	2	2	A = A ⊕ op	N . . . . . Z C
69	EOR	dp	A5	2	3	˝	N . . . . . Z C
70	EOR	dp+X	A6	2	4	˝	N . . . . . Z C
71	EOR	!abs	A7	3	4	˝	N . . . . . Z C
72	EOR	!abs+Y	B5	3	5	˝	N . . . . . Z C
73	EOR	[dp+X]	B6	2	6	˝	N . . . . . Z C
74	EOR	[dp]+Y	B7	2	6	˝	N . . . . . Z C
75	EOR	{X}	B4	1	3	˝	N . . . . . Z C
76	INC	A	88	1	2	OP = OP + 1	N . . . . . Z C
77	INC	dp	89	2	4	˝	N . . . . . Z C
78	INC	dp + X	99	2	5	˝	N . . . . . Z C
79	INC	!abs	98	3	5	˝	N . . . . . Z C
80	INC	X	8F	1	2	˝	N . . . . . Z C
81	INC	Y	9E	1	2	˝	N . . . . . Z C
82	JMP	!abs	1B	3	3	Branch	. . . . .
83	JMP	[!abs]	1F	3	5	˝	. . . . .
84	JMP	[dp]	3F	2	4	˝	. . . . .
85	CALL	!abs	3B	3	8	Subroutine call	. . . . .
86	CALL	[dp]	5F	2	8	˝	. . . . .
87	PCALL	upage	4F	2	6	˝	. . . . .
88	TCALL	n	nA	1	8	˝	. . . . .

No.	MNEMONIC		OP CODE	Words	Exec. Cycle	OPERATION	Flag MVG HIZC
89	LDA	#imm	C4	2	2	A = op	N . . . . . Z .
90	LDA	dp	C5	2	3	˝	N . . . . . Z .
91	LDA	dp+X	C6	2	4	˝	N . . . . . Z .
92	LDA	!abs	C7	3	4	˝	N . . . . . Z .
93	LDA	!abs+Y	D5	3	5	˝	N . . . . . Z .
94	LDA	[dp+X]	D6	2	6	˝	N . . . . . Z .
95	LDA	[dp]+Y	D7	2	6	˝	N . . . . . Z .
96	LDA	{X}	D4	1	3	˝	N . . . . . Z .
97	LDA	{X}+	DB	1	4	A = op, X = X+1	N . . . . . Z .
98	LDA	dp, #imm	E4	3	5	dp = $\overline{\text{imm}}$	. . . . .
99	LDX	#imm	1E	2	2	X = op	N . . . . . Z .
100	LDX	dp	CC	2	3	v	N . . . . . Z .
101	LDX	dp+Y	CD	2	4	v	N . . . . . Z .
102	LDX	!abs	DC	3	4	v	N . . . . . Z .
103	LDY	#imm	3E	2	2	Y = op	N . . . . . Z .
104	LDY	dp	C9	2	3	v	N . . . . . Z .
105	LDY	dp+X	D9	2	4	v	N . . . . . Z .
106	LDY	!abs	D8	3	4	v	N . . . . . Z .
107	LSR	A	48	1	2	op = op >>1	N . . . . . Z C
108	LSR	dp	49	2	4	v	N . . . . . Z C
109	LSR	dp + X	59	2	5	v	N . . . . . Z C
110	LSR	!abs	58	3	5	v	N . . . . . Z C
111	MUL		5B	1	9	YA = Y * A	N . . . . . Z .
112	NOP		FF	1	2	No operation	. . . . .
113	OR	#imm	64	2	2	A = A : op	N . . . . . Z .
114	OR	dp	65	2	3	˝	N . . . . . Z .
115	OR	dp+X	66	2	4	˝	N . . . . . Z .
116	OR	!abs	67	3	4	˝	N . . . . . Z .
117	OR	!abs+Y	75	3	5	˝	N . . . . . Z .
118	OR	[dp+X]	76	2	6	˝	N . . . . . Z .
119	OR	[dp]+Y	77	2	6	˝	N . . . . . Z .
120	OR	{X}	74	1	3	˝	N . . . . . Z .
121	PUSH	A	0E	1	4	Push op, SP = SP - 1	. . . . .
122	PUSH	X	2E	1	4	˝	. . . . .
123	PUSH	Y	4E	1	4	˝	. . . . .
124	PUSH	PSW	6E	1	4	˝	. . . . .
125	POP	A	0D	1	4	Pop op, SP = SP + 1	. . . . .
126	POP	X	2D	1	4	˝	. . . . .
127	POP	Y	4D	1	4	˝	. . . . .
128	POP	PSW	6D	1	4	˝	(restored)
129	ROL	A	28	1	2	op = op << 1, with C	N . . . . . Z C
130	ROL	dp	29	2	4	˝	N . . . . . Z C
131	ROL	dp+X	39	2	5	˝	N . . . . . Z C
132	ROL	!abs	38	3	5	˝	N . . . . . Z C
133	ROR	A	68	1	2	op = op >> 1, with C	N . . . . . Z C
134	ROR	dp	69	2	4	˝	N . . . . . Z C
135	ROR	dp+X	79	2	5	˝	N . . . . . Z C
136	ROR	!abs	78	3	5	˝	N . . . . . Z C

APPENDIX.C

No.	MNEMONIC		OP CODE	Words	Exec. Cycle	OPERATION	Flag MVG HIZC
137	RETI		7F	1	6	Interrupt end	(restored)
138	RET		6F	1	5	Subroutine end	. . . . .
139	SBC	#imm	24	2	2	A = A - op - C	N V . . H . Z C
140	SBC	dp	25	2	3	″	N V . . H . Z C
141	SBC	dp+X	26	2	4	″	N V . . H . Z C
142	SBC	!abs	27	3	4	″	N V . . H . Z C
143	SBC	!abs+Y	35	3	5	″	N V . . H . Z C
144	SBC	[dp+X]	36	2	6	″	N V . . H . Z C
145	SBC	[dp]+Y	37	2	6	″	N V . . H . Z C
146	SBC	{X}	34	1	3	″	N V . . H . Z C
147	SETI	dp.bit	x1	2	4	op.bit = 1	. . . . .
148	SETA1	A.bit	0B	2	2	″	. . . . .
149	SETC		A0	1	2	C = 1	 1
150	SETG		C0	1	2	G = 1	. . 1 . . . .
151	SLEEP		00	1	3	CPU stop	. . . . .
152	STA	dp	E5	2	4	op = A	. . . . .
153	STA	dp+X	E6	2	5	″	. . . . .
154	STA	!abs	E7	3	5	″	. . . . .
155	STA	!abs+Y	F5	3	6	″	. . . . .
156	STA	[dp+X]	F6	2	7	″	. . . . .
157	STA	[dp]+Y	F7	2	7	″	. . . . .
158	STA	{X}	F4	1	4	″	. . . . .
159	STA	{X}+	FB	1	4	op = A, X=X+1	. . . . .
160	STOP		EF	1	3	CPU, OSC stop	. . . . .
161	STX	dp	EC	2	4	op = X	. . . . .
162	STX	dp+Y	ED	2	5	″	. . . . .
163	STX	!abs	FC	3	5	″	. . . . .
164	STY	dp	E9	2	4	op = Y	. . . . .
165	STY	dp+X	F9	2	5	″	. . . . .
166	STY	!abs	F8	3	5	″	. . . . .
167	TAX		E8	1	2	X= A	N . . . . Z .
168	TAY		9F	1	2	Y = A	N . . . . Z .
169	TST	dp	4C	2	3	Test dp = 0 or not	N . . . . Z .
170	TSPX		AE	1	2	X = SP	N . . . . Z .
171	TXA		C8	1	2	A = X	N . . . . Z .
172	TXSP		8E	1	2	SP = X	. . . . .
173	TYA		BF	1	2	A = Y	N . . . . Z .
174	XAX		EE	1	4	A ↔ X	. . . . .
175	XAY		DE	1	4	A ↔ Y	. . . . .
176	XCN		CE	1	5	A7-4 A3-0	N . . . . Z .
177	XMA	dp	BC	2	5	A ↔ op	N . . . . Z .
178	XMA	dp+X	AD	2	6	″	N . . . . Z .
179	XMA	{X}	BB	1	5	″	N . . . . Z .
180	XYX		FE	1	4	X ↔ Y	. . . . .

No.	MNEMONIC		OP CODE	Words	Exec. Cycle	OPERATION	Flag MVG HIZC
181	LDYA	dp	7D	2	5	YA = (dp+1)(dp)	N . . . . . Z .
182	STYA	dp	DD	2	5	(dp+1)(dp) = YA	. . . . .
183	INCW	dp	9D	2	6	(dp+1)(dp)++	N . . . . . Z .
184	DECW	dp	BD	2	6	(dp+1)(dp)--	N . . . . . Z .
185	ADDW	dp	1D	2	5	YA + (dp+1)(dp)	N V . . H . Z C
186	SUBW	dp	3D	2	5	YA - (dp+1)(dp)	N V . . H . Z C
187	CMPW	dp	5D	2	4	CP YA, (dp+1)(dp)	N . . . . . Z C
188	CBNE	dp, rel	FD	3	5/7	if (op !=A)	. . . . .
189	CBNE	dp+X, rel	8D	3	6/8	then branch	. . . . .
190	DBNE	dp, rel	AC	3	5/7	Dec op, if (Z=0)	. . . . .
191	DBNE	Y, rel	7B	2	4/6	then branch	. . . . .
192	NOT1	M.bit	4B	3	5	M.bit = $\overline{\text{M.bit}}$	. . . . .
193	OR1	M.bit	6B	3	5	C = M.bit : C	 C
194	OR1B	M.bit	6B	3	5	C = ($\overline{\text{M.bit}}$) : C	 C
195	AND1	M.bit	8B	3	4	C = M.bit & C	 C
196	AND1B	M.bit	8B	3	4	C = ($\overline{\text{M.bit}}$) & C	 C
197	EOR1	M.bit	AB	3	5	C= M.bit $\oplus$ C	 C
198	EOR1B	M.bit	AB	3	5	C = ($\overline{\text{M.bit}}$) $\oplus$ C	 C
199	LDC	M.bit	CB	3	4	C = M.bit	 C
200	LDCB	M.bit	CB	3	4	C = ($\overline{\text{M.bit}}$)	 C
201	STC	M.bit	EB	3	6	M.bit = C	. . . . .
202	TCLR1	!abs	5C	3	6	!abs = A & !abs	N . . . . . Z .
203	TSET1	!abs	3C	3	6	!abs = A : !abs	N . . . . . Z .

APPENDIX.D INSTRUCTION MAP

	0000 (0)	0001 (1)	0010 (2)	0011 (3)	0100 (4)	0101 (5)	0110 (6)	0111 (7)	1000 (8)	1000 (8)	1010 (A)	1011 (B)	1100 (C)	1101 (D)	1110 (E)	1111 (F)
0000 (0)	SLEEP	SET1 dp.bit	BBS A.bit	BBS dp.bit	ADC imm	ADC dp	ADC dp+x	ADC !abs	0000 (0)	ASL A	TCAKK 0	STEA!	BIT dp	POP A	PUSHA	BRK
0001 (1)	BPL	CLR1 dp.bit	BBC A.bit	BBC dp.bit	ADC {X}	ADC !abs+Y	ADC [dp+X]	ADC [dp]+Y	0000 (0)	ASL !abs	TCAKK 1	JMP !ABS	BIT !abs	ADDW dp	LDX imm	JMP [!abs]
0010 (2)	CLRC	SET1 dp.bit	BBS A.bit	BBS dp.bit	SBC imm	SBC dp	SBC dp+x	SBC !abs	0000 (0)	ROL A	TCAKK 2	CLRA1	COM dp	POP X	PUSH X	BRA
0011 (3)	SVC	CLR1 dp.bit	BBC A.bit	BBC dp.bit	SBC {X}	SBC !abs+Y	SBC [dp+X]	SBC [dp]+Y	0000 (0)	ROL !abs	TCAKK 3	CALL !abs	TEST1 !abs	SUBW dp	LDY imm	JMP [dp]
0100 (4)	CLRG	SET1 dp.bit	BBS A.bit	BBS dp.bit	CMP imm	CMP dp	CMP DP+X	CMP !abs	0000 (0)	LSR A	TCAKK 4	NOT1	TST dp	POP Y	PUSH Y	PCALL
0101 (5)	BCC	CLR1 dp.bit	BBC A.bit	BBC dp.bit	CMP {X}	CMP !abs+Y	CMP [dp+X]	CMP [dp]+Y	0000 (0)	LSR !abs	TCAKK 5	MUL	TCLR1 !abS	CMPW dp	CMPX imm	CALL [dp]
0110 (6)	DI	SET1 dp.bit	BBS A.bit	BBS dp.bit	OR imm	OR dp	OR dp+X	OR !abs	0000 (0)	ROR A	TCAKK 6	OR1 OR1B	CMPX dp	POP PSW	PUSH PSW	RET
0111 (7)	BNE	CLR1 dp.bit	BBC A.bit	BBC dp.bit	OR {X}	OR dp	OR dp+X	OR !abs	0000 (0)	ROR !abs	TCAKK 7	DBNE Y	CMPX !abs	LDYA dp	CMPY imm	RETI
1000 (8)	CLRV	SET1 dp.bit	BBS A.bit	BBS dp.bit	AND imm	AND dp	AND dp+X	AND !abs	0000 (0)	INC A	TCAKK 8	AND1 AND1B	CMPY dp	CBNE dp+X	TXSP	INC X
1001 (9)	BMI	CLR1 dp.bit	BBC A.bit	BBC dp.bit	AND {X}	AND !abs+Y	AND [dp+X]	AND [dp]+Y	0000 (0)	INC !abs	TCAKK 9	DIV	CMPY !abs	INCW dp	INC Y	TAY X
1010 (A)	SETC	SET1 dp.bit	BBS A.bit	BBS dp.bit	EOR imm	EOR dp	EOR pd+X	EOR !abs	0000 (0)	DEC A	TCAKK 10	EOR1 EOR1B	DBNE dp	XMA dp+X	TSPX	DEC X
1011 (B)	BVS	CLR1 dp.bit	BBC A.bit	BBC dp.bit	EOR {X}	EOR !abs+Y	EOR [dp+X]	EOR [dp]+Y	0000 (0)	DEC !abs	TCAKK 11	XMA {X}	XMA dp+X	DECW dp	DEC Y	TYA
1100 (C)	SETG	SET1 dp.bit	BBS A.bit	BBS dp.bit	LDA imm	LDA dp	LDA dp+X	LDA !abs	0000 (0)	TXA	TCAKK 12	LDC LDCB	LDX dp	LDX dp+Y	XCN	DAS
1101 (D)	BCS	CLR1 dp.bit	BBC A.bit	BBC dp.bit	LAD {X}	LDA !abs+Y	LDA [dp+X]	LDA [dp]+Y	0000 (0)	LDY !abs	TCAKK 13	LDA {X}+	LDX !abs	STYA dp	XAY	DAA
1110 (E)	EI	SET1 dp.bit	BBS A.bit	BBS dp.bit	LDM dp	STA dp	STA !dp+X	STA !abs	0000 (0)	TAX	TCAKK 14	STC	STX dp	STX dd+Y	XAX	STOP
1111 (F)	BEQ	CLR1 dp.bit	BBC A.bit	BBC dp.bit	STA {X}	STA !abs+y	STA [dp]+Y	STA [dp]+Y	0000 (0)	STY !abs	TCAKK 15	STA {X}=	STX !abs	CBNE dp	XYX	NOP

APPENDIX.E RAMINIT.H

```
;
;=========================================================================
;       DEFINE  PORT  &  REGISTER  ADDRESS
;=========================================================================
;
R0              EQU    0C0H             ;PORT R0 REG.
R0DD            EQU    0C1H             ;PORT R0 DATA I/O DIRECTION REG.
R1              EQU    0C2H             ;PORT R1 REG.
R1DD            EQU    0C3H             ;PORT R1 DATA I/O DIRECTION REG.
R2              EQU    0C4H             ;PORT R2 REG.
R2DD            EQU    0C5H             ;PORT R2 DATA I/O DIRECTION REG.
TMR             EQU    0C6H             ;TEST MODE REG.
CLKCTR          EQU    0C7H             ;CLOCK CONTROL REG.
BITR            EQU    0C7H             ;BASIC INTERVAL TIMER REG.
WDTR            EQU    0C8H             ;WATCH DOG TIMER REG.
PMR1            EQU    0C9H             ;PORT R1 MODE REG.
IMOD            EQU    0CAH             ;INT. MODE REG.
IEDS            EQU    0CBH             ;EXTERNAL INT. EDGE SELECTION
;
IENL            EQU    0CCH             ;INT. ENABLE REG. LOW
IWWDT           EQU    6,0CCH           ;W.D.T. INT. ENABLE
IEBIT           EQU    5,0CCH           ;B.I.T. INT. ENABLE
;
IRQL            EQU    0CDH             ;INT. REQUEST FLAG REG. LOW
IRQWDT          EQU    6,0CDH           ;W.D.T. INT. REQUEST FLAG
IRQBIT          EQU    5,0CDH           ;B.I.T. INT. REQUEST FLAG
;
IENH            EQU    0CEH             ;INT. ENABLE REG. HIGH
IEKSCN          EQU    7,0CEH           ;EXTERNAL INT.0 ENABLE
IEE1            EQU    6,0CEH           ;EXTERNAL INT.1 ENABLE
IEE2            EQU    5,0CEH           ;EXTERNAL INT.2 ENABLE
IET0            EQU    3,0CEH           ;TIMER0 INT. ENABLE
IET1            EQU    2,0CEH           ;TIMER1 INT. ENABLE
IET2            EQU    1,0CEH           ;TIMER2 INT. ENABLE
;
IRQH            EQU    0CFH             ;INT. REQUEST FLAG REG. HIGH
IRQKSCN         EQU    7,0CFH           ;EXTERNAL INT.0 REQUEST FLAG
IRQE1           EQU    6,0CFH           ;EXTERNAL INT.1 REQUEST FLAG
IRQE2           EQU    5,0CFH           ;EXTERNAL INT.2 REQUEST FLAG
IRQT0           EQU    3,0CFH           ;TIMER0 INT. REQUEST FLAG
IRQT1           EQU    2,0CFH           ;TIMER1 INT. REQUEST FLAG
IRQT2           EQU    1,0CFH           ;TIMER2 INT. REQUEST FLAG ;
```

```
;
TM0         EQU   0D0H          ;TIMER0 MODE REG.
CAP0        EQU   7,0D0H        ;TIMER0 INTERRUPT SEL.
T0ST        EQU   6,0D0H        ;TIMER0 START
T0CN        EQU   5,0D0H        ;TIMER0 CONTINUOUS
T0MOD       EQU   4,0D0H        ;TIMER0 SINGLE/MODULO SEL.
T0IFS       EQU   3,0D0H        ;TIMER0 EVERY/TWICE SEL.
T0SL2       EQU   2,0D0H        ;TIMER0 CLOCK SEL. 2
T0SL1       EQU   1,0D0H        ;TIMER0 CLOCK SEL. 1
T0SL0       EQU   0,0D0H        ;TIMER0 CLOCK SEL. 0
;
TM1         EQU   0D1H          ;TIMER1 MODE REG.
T1ST        EQU   7,0D1H        ;TIMER1 START
T1CN        EQU   6,0D1H        ;TIMER1 CONTINUOUS
T1MOD       EQU   5,0D1H        ;TIMER1 MODULO/SINGLE SEL.
T1IFS       EQU   4,0D1H        ;TIMER1 EVERY/TWICE SEL.
T1SL2       EQU   2,0D1H        ;TIMER1 CLOCK SEL. 2
T1SL1       EQU   1,0D1H        ;TIMER1 CLOCK SEL. 1
T1SL0       EQU   0,0D1H        ;TIMER1 CLOCK SEL. 0
;
TM2         EQU   0D2H          ;TIMER2 MODE REG.
T2ST        EQU   4,0D2H        ;TIMER2 START
T2CN        EQU   3,0D2H        ;TIMER2 CONTINUOUS
T2SL2       EQU   2,0D2H        ;TIMER2 CLOCK SEL. 2
T2SL1       EQU   1,0D2H        ;TIMER2 CLOCK SEL. 1
T2SL0       EQU   0,0D2H        ;TIMER2 CLOCK SEL. 0
;
T0HMD       EQU   0D3H          ;TIMER0 HIGH MSB DATA REG.
T0HLD       EQU   0D4H          ;TIMER0 HIGH LSB DATA REG.
T0LMD       EQU   0D5H          ;TIMER0 LOW MSB DATA REG.
T0LLD       EQU   0D6H          ;TIMER0 LOW LSB DATA REG.
T1HD        EQU   0D7H          ;TIMER1 HIGH DATA REG.
T1LD        EQU   0D8H          ;TIMER1 LOW DATA REG.
T2DR        EQU   0D9H          ;TIMER2 DATA REG.
;
TM01        EQU   0DAH          ;TIMER0 / TIMER1 MODE REG.
TOUTS       EQU   7,0DAH        ;REMOUT PORT OUTPUT SEL.
TOUTB       EQU   6,0DAH        ;REMOUT PORT BIT CONTROL
T0OUTP      EQU   4,0DAH        ;TIMER0 POLARITY SEL.
T0INIT      EQU   3,0DAH        ;TIMER0 OUTPUT INIT. VALUE
T1INIT      EQU   2,0DAH        ;TIMER1 OUTPUT INIT. VALUE
TOUT1       EQU   1,0DAH        ;TIMER1 OUTPUT LOGIC
TOUT0       EQU   0,0DAH        ;TIMER0 OUTPUT LOGIC
;
SMRR0       EQU   0DCH          ;STANBY MODE RELEASE REG.0
SMRR1       EQU   0DDH          ;STANBY MODE RELEASE REG.1
R1ODC       EQU   0DEH          ;PORT R1 OPEN DRAIN ASSIGN REG.
;=====================================================================
;
```

APPENDIX.F Noise reduction on the PCB

Countermeasures Against Noise During Transmission of Carrier Output

When a signal is transmitted from the transmitter of a remote controller, a peak current of 0.5~1A may flow through the infrared LED. Since two batteries are usually used as the power source of the transmitter, equivalent resistance (R) exists in the power source. (See below example circuit)
This resistance (R) increases to 10~20Ω if the supply voltage drops to 2V.
While the carrier is output from the REMOUT PIN, a high-frequency noise may be generated on the power lines due to the voltage fluctuation that may take place especially during switching. To minimize the influence on the microcontroller of this high-frequency noise, take the following measures:

① Separate the power lines of the microcontroller from the power line of the infrared LED with the terminals of the batteries at the center. Use thick power lines and keep the wiring short (resistors must not to be used at the power lines of the microcontroller)
② Locate the oscillator as close as possible to the microcontroller and shield it with GND lines (Shaded portion in the figure below)
③ Locate the capacitor for stabilization of the power supply closely to the power lines of the microcontroller. Also, it is useful to use a capacitor to eliminate high-frequency noise.